

***SERVICE MANUAL***

**C286-LT**

**OCTOBER, 1990**

**PN-400400-01**



***Produced By:***

**Commodore International Spare Parts GmbH  
Braunschweig, West Germany**

***SERVICE MANUAL***

**C286-LT**

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***INTERNATIONAL EDITION***

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**SECTION 1**  
**SPECIFICATIONS**

## 1.1 TECHNICAL SPECIFICATIONS

### C286-LT

### AT Compatible

#### MEMORY

RAM on board

1MB: 640 KB Base memory, 384 KB extended/expanded memory; configurable by user

VIDEO RAM

256 KB (A000:0000H-13000;FFFFH): 32 KB (frame buffer for LCD)

ROM

128 KB (64 KB for system BIOS, 64 KB for VGA video BIOS)

#### RAM EXPANDABLE

on board

Yes; to 5M — 2 meg. memory expansion cards optional (maximum of two cards for a total of 5 meg.)

#### CPU

Type

80C286

Clock speed

12.5 MHz, 8 MHz

#### EXTERNAL STORAGE

##### Floppy disk drive

Type

3.5-inch double-sided high density

Supported disks

3.5-inch 1.4 MB, 3.5-inch 720 KB

##### Hard disk

Capacity

20 MB

Type

2.5-inch, low power consumption type

Access time

23 ms mean access time

Interface

IDE

#### DISPLAY

Dimensions

197 mm x 149 mm (7 $\frac{3}{4}$ " x 5 $\frac{7}{8}$ ") diagonal 247 mm (9 $\frac{3}{4}$ ")  
0.27 mm dots size and 0.3 mm dot pitch  
1:1 aspect ratio

Type

STN type LCD with CFL backlight lamp

Video mode

Compatible with VGA

Text: 80 characters x 25 lines or 40 characters x 25 lines

Graphics: 640 x 480

Gray scale

8 shades of gray

#### AC ADAPTER

Input

Operating voltage — 100 to 240 VAC

Frequency — 50/60 Hz

Output power

Adapter mode — 24 W

Charger mode — 45 W

Input current

Adapter mode — 0.6 A

Charger mode — 1 A

Dimensions

85 W x 205 D x 55 H mm

Weight

0.65 Kg

#### SOFTWARE

Operating System

MS-DOS 4.01 with Shell

Language

GW-BASIC

##### Utilities

Eagle.com

LCD control

Switcher.com

LCD control

Alarm.com

Indicating low battery

Mdmon.com/mdmoff.com

Modem power on/off

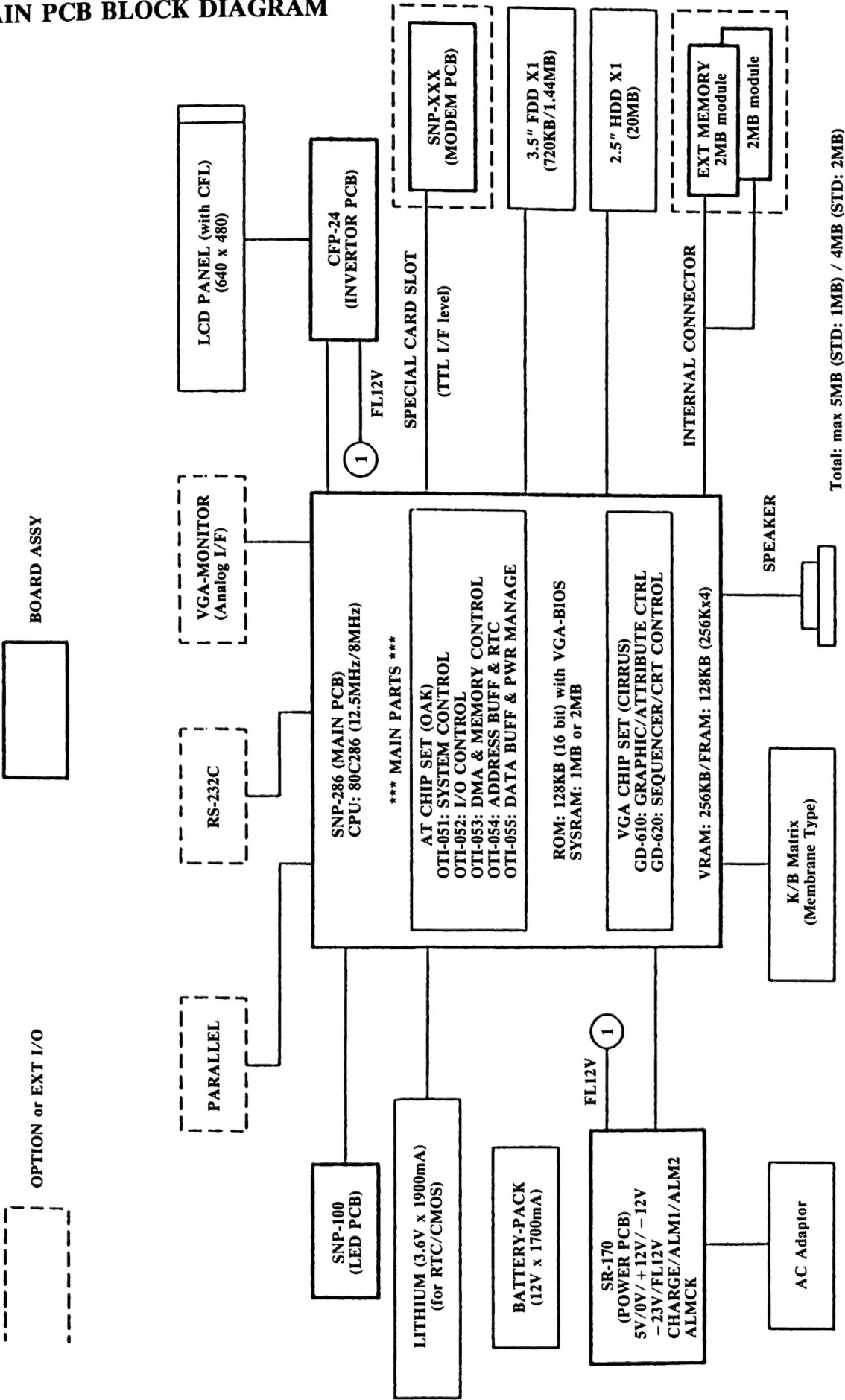
**SECTION 2**

**THEORY OF OPERATIONS**

***NOTE***

**PLEASE REFER TO C286-LT OPERATIONS MANUAL  
PN-363573-01 FOR ADDITIONAL INFORMATION**

2.1 MAIN PCB BLOCK DIAGRAM



2.1 — MAIN PCB BLOCK DIAGRAM

## 2.2 MAIN SYSTEM PARTS

**SYSTEM CONTROL** OTI-051

**I/O CONTROL** OTI-052

**DMA & MEMORY CONTROL** OTI-053

**ADDRESS BUFFER & RTC** OTI-054

**DATA BUFFER & POWER MANAGER** OTI-055

**SYSTEM CLOCK** OTI-051

### **DMA CHANNEL ASSIGNMENT**

Channel 0 - Not used  
 Channel 1 - Not used  
 Channel 2 - Floppy Disk Controller  
 Channel 3 - 4 Not used  
 Channel 5 - 7 Not used

**INTERRUPT CONTROL** OTI-052

### **INTERRUPT CONTROLLER CHANNEL ASSIGNMENT**

IRQ 0 - Timer Channel 0  
 IRQ 1 - Keyboard Interface Interrupt  
 IRQ 2 - Not used  
 IRQ 3 - Com2 Interrupt  
 IRQ 4 - Com1 Interrupt  
 IRQ 5 - Not used  
 IRQ 6 - Floppy Disk Controller Interrupt  
 IRQ 7 - Printer Interface Interrupt  
 IRQ 8 - Real Time Clock  
 IRQ 9 - Not used  
 IRQ10 - Power Saving Mode  
 IRQ11 - 13 Not used  
 IRQ14 - Hard Disk Controller Interrupt  
 IRQ15 - Not used

**BUS CONTROLLER** OTI - 051

**TIMER/COUNTER** OTI - 052

### **TIMER/COUNTER CHANNEL ASSIGNMENT**

Channel 0 - System Timer for use with MS-DOS  
 Channel 1 - Memory Refresh Timing Generator  
 Channel 2 - Speaker Beep Tone Generator

**KEYBOARD/SENSE CONTROL PORT** 80C42

### **OUTLINE OF OTI-051**

The OTI-051 is a customized IC in the Oak Model 35 chip set and it is a system control chip used in IBM AT and Model 30-286 architectures. Its main features are described below.

<b>System Control</b>	8 MHz, 10 MHz, 12.5 MHz, 16 MHz and 20 MHz system speeds supported
<b>I/O Channels</b>	8 MHz asynchronous mode, and 8 MHz, 10 MHz and 12 MHz synchronous modes Programmable wait state
<b>Laptop</b>	Power management function
<b>Other Features</b>	Fast reset and time-out counter



**2.2 MAIN SYSTEM PARTS (Continued)****OUTLINE OF OTI-052**

The OTI-052 is an I/O peripheral controller circuit which comes with the following functions.

- Two 8259-compatible interrupt controllers
- 8254-compatible timer/counter
- 16450-compatible serial communication controller
- Floppy disk controller, hard disk subsystem, keyboard controller, numerical calculation processor and other chip select circuits
- Numerical calculation processor interface circuit

**OUTLINE OF OTI-053 DMA & MEMORY CONTROLLERS**

The OTI-053 is an integrated circuit which has a DMA controller and memory controller, and its main features are listed below.

- 0 wait cycle page mode and interleave mode
- DRAMs with access times ranging from 60ns to 120ns supported
- System speeds up to a maximum 20 MHz
- Programmable wait state for slow-speed DRAMs
- Non-wait state ROM cycle execution enabled with use of shadow RAM
- EMS4.0 supported
- 640KB system memory and total memory space of up to 8MB using extension/expansion memories supported
- 256KB and 1MB type DRAMs supported
- Dummy SRAM for laptop models supported
- Cartridge ROMs supported

**DMA Control**

- Fast and normal DMA modes with built-in 8237 to handle operating speeds up to 10 MHz

**Laptop Support**

- Power-saving mode

**OUTLINE OF OTI-054**

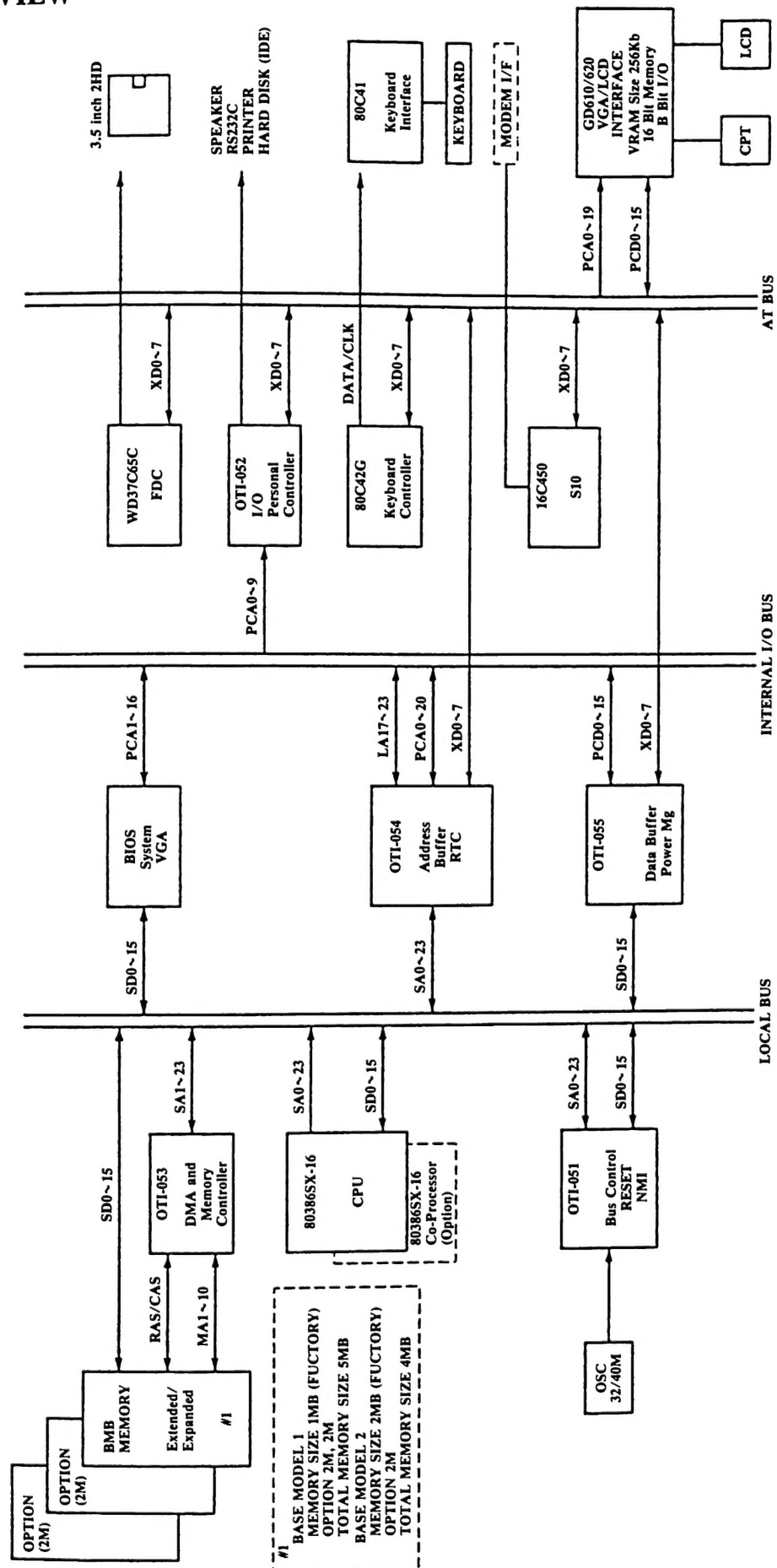
The OTI-054 is a customized IC in the Oak Model 35 chip set and it is an address buffer driver for IBM AT, Model 30 and other 286-compatible systems. It features all the TTL address and command driver functions normally required on a system board. In addition to its address driver functions, it comes with an RTC (real-time clock) function. Except for the 3 items below, the RTC function is compatible with the MC146818.

- 128-byte CMOS RAM in total
- No CKFS (clock-out frequency select) input facility
- No SQW (square wave) output facility

**OUTLINE OF OTI-055**

The OTI-055 features all the TTL data driver functions normally required on a system board and, in addition to its data buffer functions, it comes with power manager functions for laptop computers. It has 16 bidirectional control/status signal lines which can be used by system designers to control power distribution to peripheral units inside a system. Besides these 16 signal lines, it features an internal timer/counter which enables the user to supply power automatically to the system.

## 2.3 SYSTEM OVERVIEW



2.2 — SYSTEM OVERVIEW

## **2.4 DISPLAY**

### **CONTROL DEVICE**

Graphics/Attributes CL-GD610; Sequencer CL-GD620

### **GRAPHIC RESOLUTION**

620 x 480 Dots

### **CHARACTER DISPLAY**

80 Character x 25 Line or 40 Character x 25 Line

### **EMULATION MODE**

CGA, EGA, MDA, and Hercules (register level)

### **DISPLAY DEVICE**

The following devices can be used:

LCD Panel; (8 GRAY SCALES); CRT with external Analog output; (64 GRAY SCALES at MDA mode); (16 colors 640 x 480); (256 colors 320 x 200)

At the boot-up, LCD Panel is always enable. You can change LCD Panel, or External CRT by Utility software (Eagle.com/Switcher .com)

**NOTE:** VGA BIOS loads the appropriate parameter, after recognizing which monitor is connected, Color or Monochrome. When power switch is turned to on and no monitor is connected, VGA BIOS sets its parameter for monochrome monitor.

### **DISPLAY CONTROL**

VGA mode

### **VIDEO RAM**

256K Bytes + frame buffer 32K Bytes

### **VIDEO RAM ACCESS**

The Video RAM can be accessed completely in the same way as accessing normal memory RAM, from CPU. Write and Read functions are freely executed without checking the status of the display control device.

### **CHARACTER GENERATOR**

Character ROM is stored in the Video Bios and used for the character display mode (US ASCII ver.).

### **BASE SYSTEM DISPLAY DEVICE**

Consists of STN LCD (blue) panel with CFL back light. In addition, the display can be switched to the analog CRT (color/monochrome) output by software.

### **AFFECTIVE DISPLAY AREA**

#### **Display Size**

197mm x 149mm

#### **Dot Size**

0.27mm x 0.17mm

#### **Dot Pitch**

0.3mm x 0.3mm

#### **Aspect Ratio**

1:1

### **CFL/LCD Auto OFF**

If you close the panel while power switch is on, the CFL and LCD Panel will be automatically shut off.

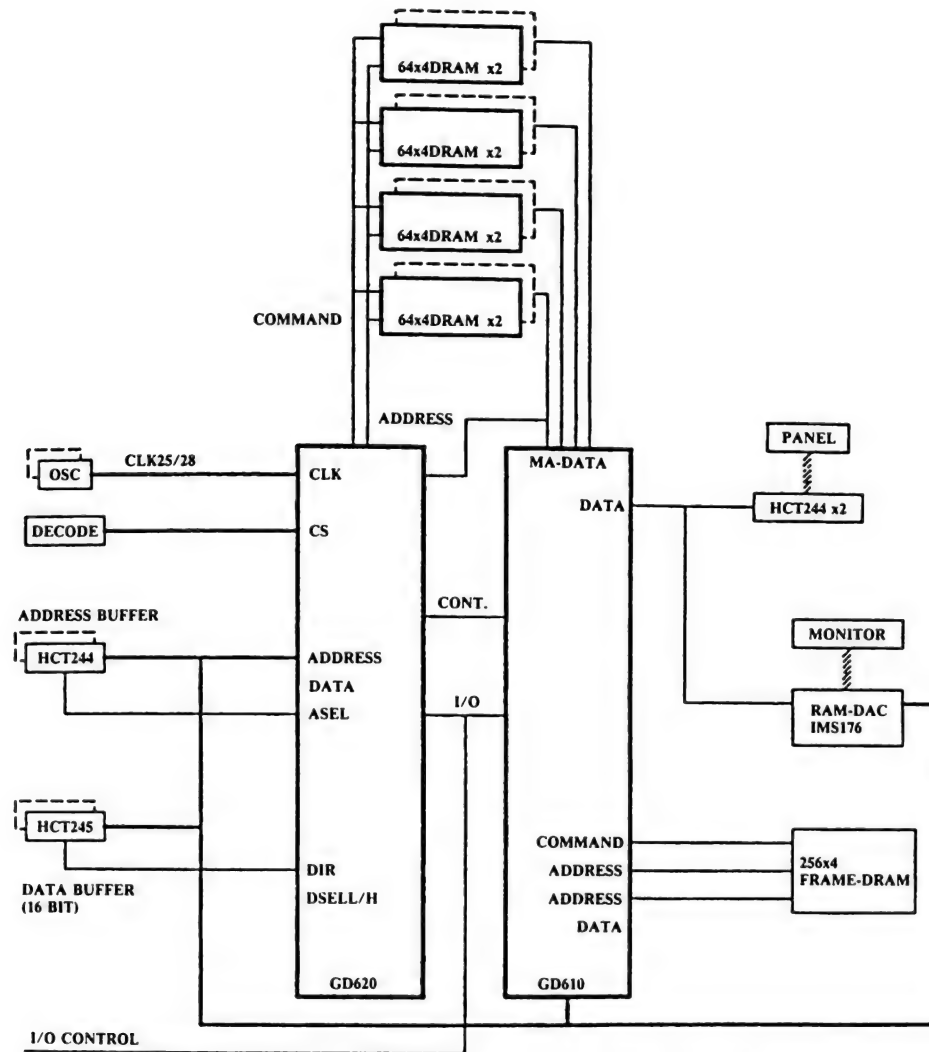
### **BACKLIGHT BRIGHTENERS**

Backlight brightness can be set high (3.2W), or LOW (1.5W) by SETUP MENU.

### **CFL BACKLIGHT LIFE**

About 8,000 hours (condition: within the max. rating)

## 2.5 VGA SYSTEM BLOCK DIAGRAM



2.3 — VGA SYSTEM BLOCK DIAGRAM

**CONNECTOR:** 15 Pin D-sub (male)

### CONNECTOR PIN ASSIGNMENT

PIN NUMBER	DESCRIPTION	PIN NUMBER	DESCRIPTION
1	Red	9	Reserved
2	Green	10	Ground
3	Blue	11	MS0*
4	MS2*	12	MS1*
5	Ground	13	Horizontal sync.
6	R Ground	14	Vertical sync.
7	G Ground	15	Not connected
8	B Ground		

\*MS0-MS2 are used for sensing a type of monitor.

## 2.6 FLOPPY DISK DRIVE AND CONTROLLER

### FLOPPY DISK DRIVE

<i>Type</i>	FD-334HF; 3.5 inch double side drive		
<i>Data Capacity</i>	1.44M/720K Bytes (formatted) 2M/1M Bytes (unformatted)		
<i>Data Transfer Rate</i>	500K bits/sec/250K bits/sec		
<i>Track Density</i>	135 tpi		
<i>Required Power</i>	+ 5V Single (4.6 - 5.5V)		
<i>Track to Track Time</i>	3msec		
<i>Disk Rotation Speed</i>	300rpm		
<i>LED Indicator</i>	Green		
<i>Width</i>	101.6mm		
<i>Height</i>	19mm		
<i>Depth</i>	135mm		
<i>Current and Power Consumption</i>		<i>Typ. current</i>	<i>Typ. power</i>
	Standby	10.0mA	50mW
	Read Operation	0.40A	2.0W
	Write Operation	0.42A	2.1W
	Motor Start	0.07A	3.5W

### FLOPPY DISK CONTROLLER

<i>Data Transmission</i>	WD37C65B
<i>Transfer Rate</i>	DMA transmit High Density — 500K bit/sec. Normal Density — 250K bit/sec.

## 2.7 HARD DISK DRIVE

<i>Type</i>	CP2024; 2.5 inch 20M Bytes Hard Disk
<i>Data Capacity</i>	21.4M Bytes (formatted)
<i>Data Transfer Rate (Media)</i>	1.25 MB/sec
<i>Data Transfer Rate (Buffer)</i>	3.75 MB/sec
<i>Seek Time</i>	Track to Track — 5ms Average — 23 ms Maximum — 40ms
<i>Rotation Speed</i>	3,433rpm
<i>Total Tracks</i>	1,306
<i>Cylinders</i>	653
<i>Disks</i>	1
<i>Data Heads</i>	2
<i>Width</i>	69.8mm
<i>Height</i>	17.5mm
<i>Length</i>	101.6mm
<i>Power Requirement</i>	+ 5V $\pm$ 5% 600mA (Typ.r/w)

## 2.8 PARALLEL PRINTER INTERFACE

### CONTROL

Printer handshaking is controlled by STROBE, and BUSY signals.

### OUTPUT

Standard TTL input printers can be used, such having TTL input. When the printer is used, the connector can be plugged in or removed without destroying the inner circuits of the devices regardless of power ON/OFF.

### PARALLEL CONNECTOR

D shell 25P (female)

### PARALLEL CONNECTOR PIN ASSIGNMENT

PIN NUMBER	DESCRIPTION	CONTENTS	
1	OUTPUT	STROBE	STROBE Signal
2	OUTPUT	PDB 0	Print data bit 0
3	OUTPUT	PDB 1	Print data bit 1
4	OUTPUT	PDB 2	Print data bit 2
5	OUTPUT	PDB 3	Print data bit 3
6	OUTPUT	PDB 4	Print data bit 4
7	OUTPUT	PDB 5	Print data bit 5
8	OUTPUT	PDB 6	Print data bit 6
9	OUTPUT	PDB 7	Print data bit 7
10	INPUT	ACK	Printer acknowledge
11	INPUT	BUSY	Printer busy
12	INPUT	P.end	Out of paper
13	INPUT	SELECT	Printer select
14	OUTPUT	ATF	Auto feed
15	INPUT	ERROR	Printer error
16	OUTPUT	INIPRN	Initialize Printer
17	OUTPUT	SELINP	Select input
18 - 25		GND	

## 2.9 RS-232C INTERFACE

**STANDARD**

EIA standard

**DEVICE**

OTI-052

**OUTPUT SIGNAL LEVEL**
Output signals based on  $\pm 12V$  supplied voltage.
**INPUT SIGNAL VOLTAGE**

SPACE = +3V, +15V

MARK = -3V, +15V

**BAUD RATE**

(50), (75), 110, 150, 300, 600, 1200, 2400, 4800, 9600

**NOTE:** The values in ( ) are not supported by software (INT 14h). They need to be directly accessed by software.

**CONNECTOR**

9 Pin D-sub (male)

**SERIAL CONNECTOR PIN ASSIGNMENT**

PIN NUMBER	SIGNAL	DESCRIPTION
1	CD	Carrier Detect
2	RxD	Receive Data
3	TxD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Signal Ground
6	DSR	Data Set Ready
7	RTS	Request To Send
8	CTS	Clear To Send
9	RI	Ring Indicator

**2.10 MODEM I/F SLOT****CONNECTOR**

20-Pin Connector Edge Socket

**STANDARD AND SIGNAL LEVEL**

Based on RS-232C, TTL Level

**MODEM CONNECTOR PIN ASSIGNMENT**

<i>PIN NUMBER</i>	<i>SIGNAL NAME</i>
A1	CONTROLLED 5 Volt
A2	CONTROLLED 5 Volt
A3	RTS
A4	DTR
A5	TXD
A6	DSR
A7	RI
A8	DCD
A9	CTS
A10	RXD
B1	- 12V
B2	GND
B3	GND
B4	GND
B5	GND
B6	GND
B7	GND
B8	GND
B9	GND
B10	GND

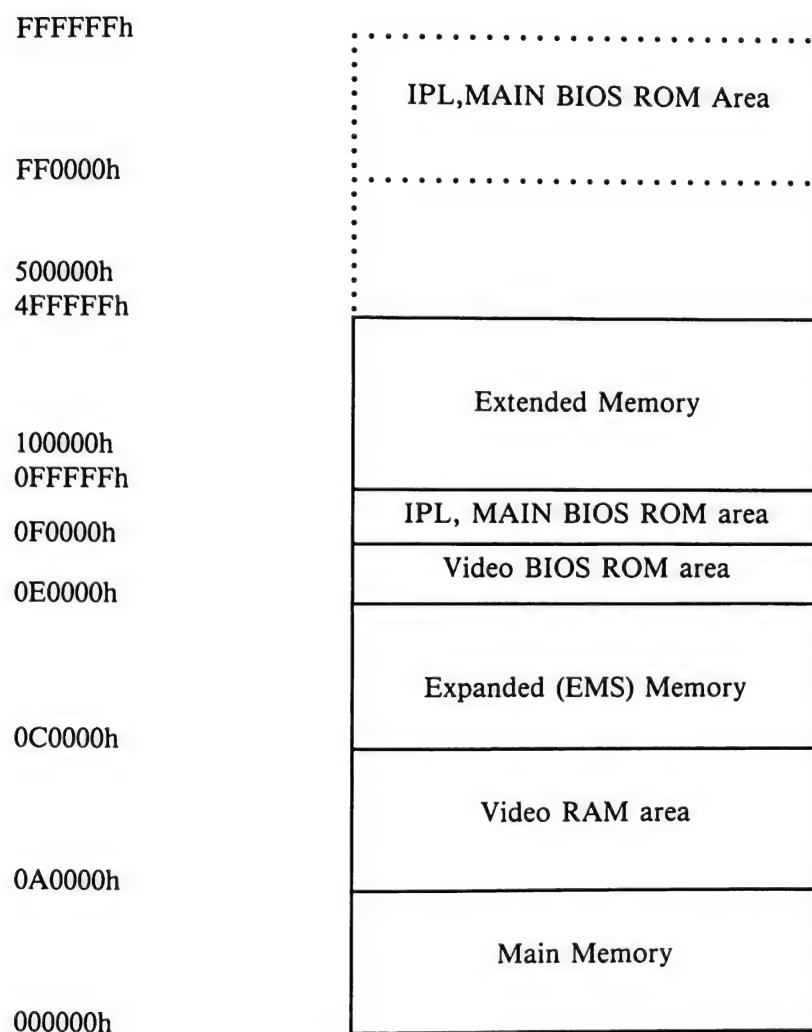


## 2.11 C286-LT MEMORY MAP

The C286-LT has available 1 MB of RAM. Base memory is 640 KB (kilobytes) and 384 KB is allocated for extended memory. By adding Commodore 2 MB RAM modules, memory may be augmented to a total of 5 MB.

By using MS-DOS 4.01 features, a portion or all extended memory can be used to emulate expanded memory conforming to the LIM 4.0 specification.

Extended memory can be utilized by many applications and operating systems functioning in protected and standard modes.



### 2.4 — MEMORY MAP

## 2.12 I/O ADDRESS MAP

<i>I/O ADDRESS</i>	<i>R/W STATUS</i>	
0000h-000Fh	R/W	DMA controller 1, 8237A
0010h-0018h	R/W	EMS register
001Eh-001Fh	R/W	OAK special register
0020h-003Fh	R/W	Interrupt controller 1, 8259A, Master
0040h-005Fh	R/W	Timer, 8254
0060h-006Fh	R/W	80C42 (Keyboard), System control register
0070h-007Fh	R/W	Real-time clock, NM1 (non-maskable interrupt) mask
0080h-008Fh	R/W	DMA page register
0094h	R/W	System board setup enable register
00A0h-00BFh	R/W	Interrupt controller 2, 8237A
00C0h-00DFh	R/W	DMA controller 2, 8237A
0102h	R/W	POS register 2
01F0h-01F7h	R/W	Fixed Disk 0
0278h-027Fh	R/W	Parallel port 3
02F8h-02FFh	R/W	Serial port 2
0378h-037Fh	R/W	Parallel port 2
03B0h-03BFh	R/W	Video Graphics Adapter 1 and Parallel port 1
03C0h-03CFh	R/W	Video Graphics Adapter 1
03D0h-03DFh	R/W	Video Graphics Adapter 1
03F0h-03F7h	R/W	Floppy Disk A
03F8h-03FFh	R/W	Serial port 1

**SECTION 3**  
**TROUBLESHOOTING**

### **3.0 TROUBLESHOOTING SECTION**

- 1) *DISASSEMBLY INSTRUCTIONS FOR FIELD REPLACEMENT UNITS***
- 2) *POWER ON DIAGNOSTIC TESTS***



**CAUTION**  
***USE ANTI-STATIC PRECAUTIONS***  
***WHEN SERVICING THIS PRODUCT***

## **DISASSEMBLY INSTRUCTIONS FOR C286-LT**

### **3.1 KEYBOARD REMOVAL INSTRUCTIONS**

Remove the three screws ① from Bottom Cabinet (the cabinet bottom). (Figure 3.1)

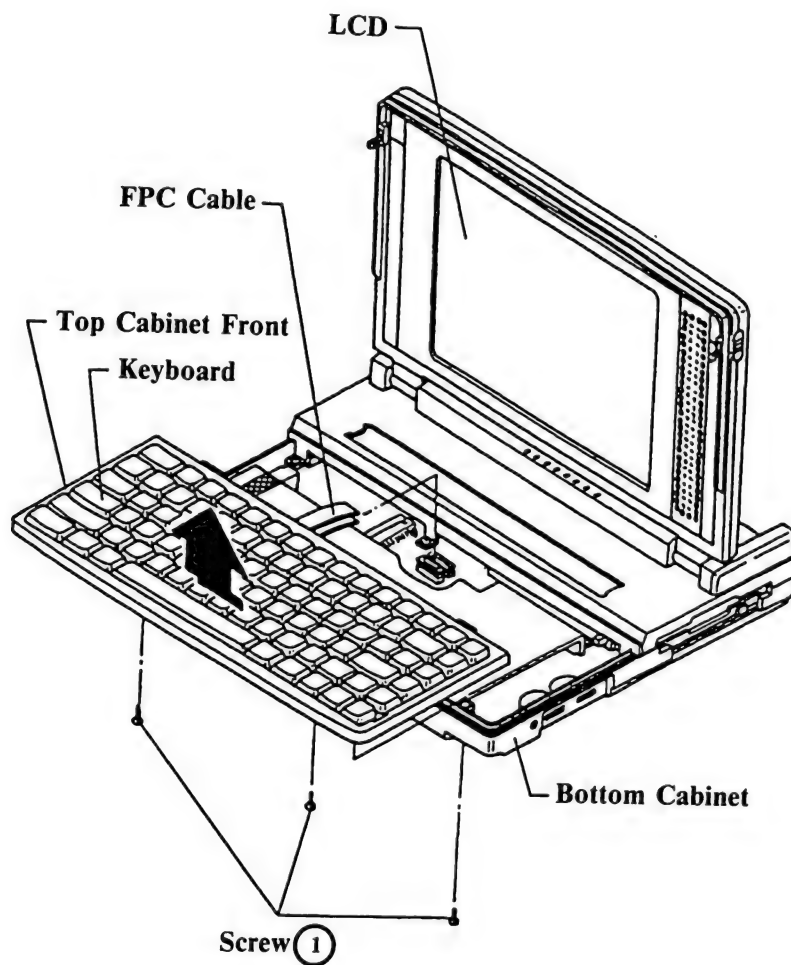
Fold up the LCD display.

Lift up Top Cabinet together with the keyboard in the direction indicated by the arrow.

**NOTE:** As the FPC cable is plugged into the connector, it must be lifted a little as well.

Unplug the FPC cable from the connector.

Remove the keyboard.



**Figure 3.1**

**DISASSEMBLY INSTRUCTIONS FOR C286-LT (Continued)**

**3.2 NICAD BATTERY PACK AND LITHIUM CELL REMOVAL INSTRUCTIONS**

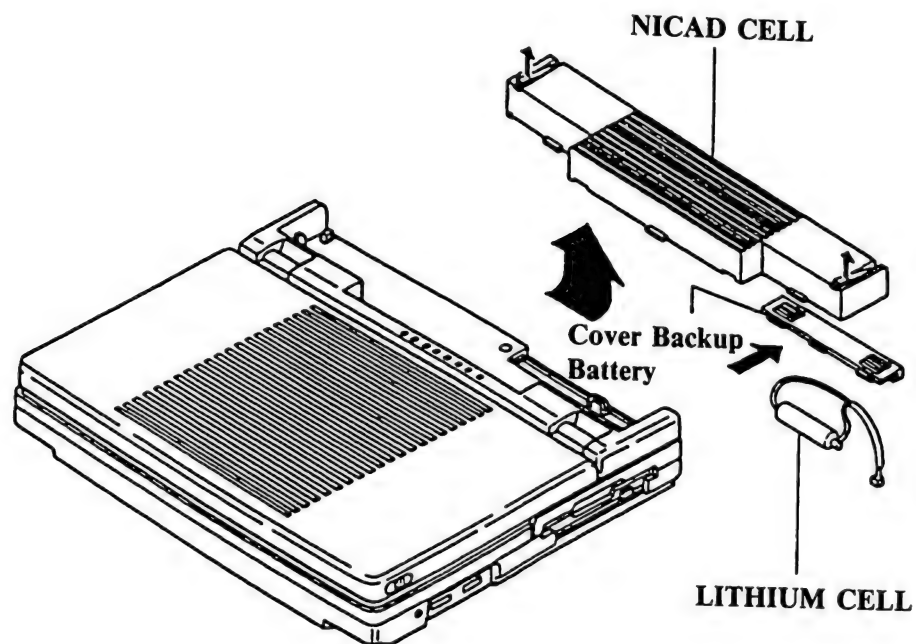
Push up on the Nicad battery pack lever in the direction indicated by the arrow. (Figure 3.2)

Remove the Nicad battery pack.

Slide Cover Backup Battery in the direction indicated by the arrow and remove it.

Take out the lithium cell and unplug the connector from it.

Remove the lithium cell.



**Figure 3.2**

**DISASSEMBLY INSTRUCTIONS FOR C286-LT (Continued)**

**3.3 HDD REMOVAL INSTRUCTIONS**

Follow the instructions under 3.1 to remove the keyboard.

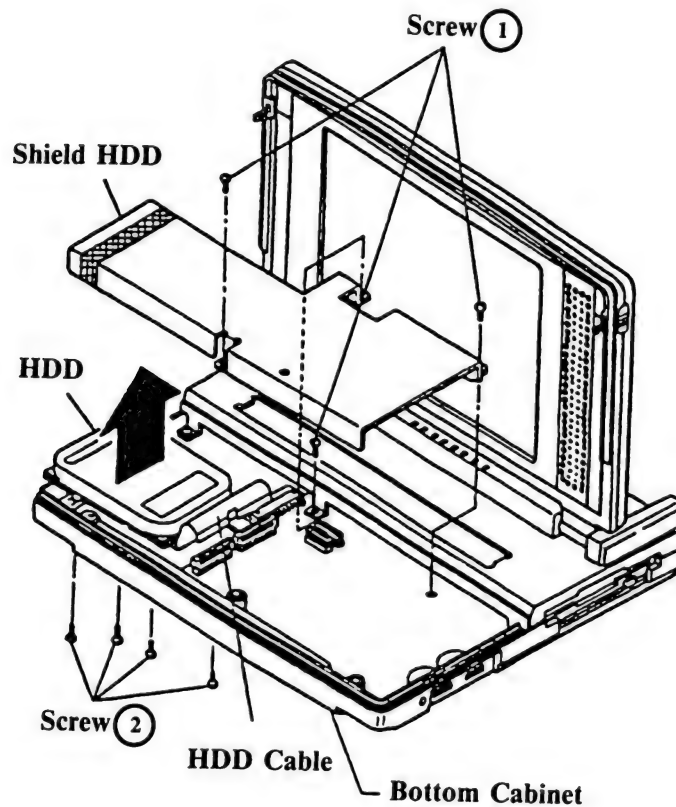
Remove the three screws (1) which hold Shield HDD in place. (Figure 3.3)

Remove Shield HDD. Do not return Shield with defect drive.

Remove the four screws (2) from Bottom Cabinet (the cabinet bottom).

Unplug the HDD cable from the connector.

Remove the HDD.



**Figure 3.3**

**DISASSEMBLY INSTRUCTIONS FOR C286-LT (Continued)****3.4 LCD POWER UNIT INVERTER REMOVAL INSTRUCTIONS**

Follow the instructions under 3.1 to remove the keyboard.

Follow step 3.2 to remove the Nicad battery pack.

Remove the six screws (1) and (2) which hold Top Cabinet Rear in place. (Figure 3.4)

Unplug connectors (1) through (9) from the main PCB. See Wiring Diagram (Figure 3.8)

Remove LCD Unit.

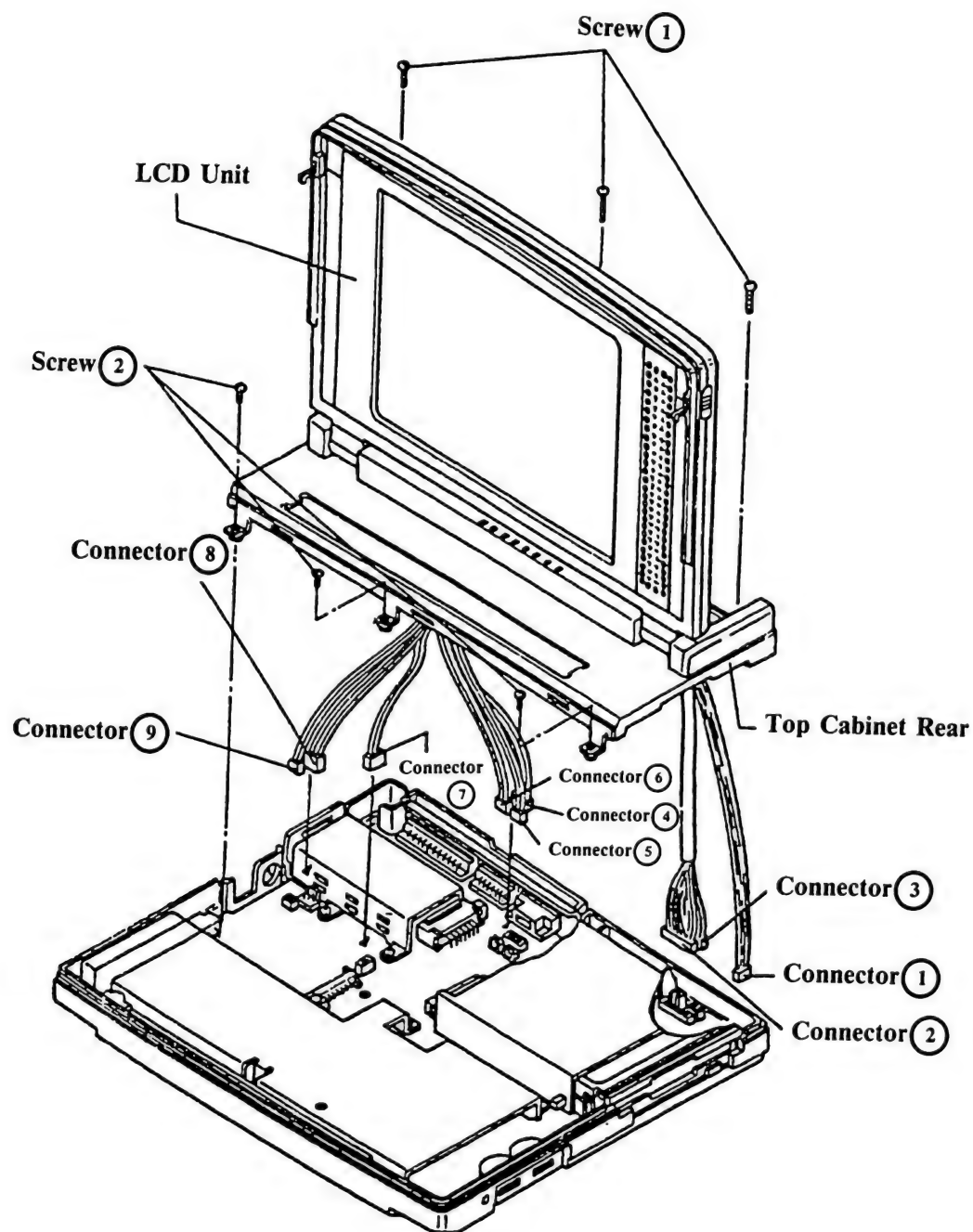


Figure 3.4



**DISASSEMBLY INSTRUCTIONS FOR C286-LT (Continued)****3.5 MAIN PCB, POWER SUPPLY PCB, FDD AND SPEAKER REMOVAL INSTRUCTIONS**

Follow the instructions under 3.1 to remove the keyboard.

Follow step 3.2 to remove the Nicad battery pack.

Follow step 3.3 to remove Shield HDD and HDD.

Follow step 3.4 to remove LCD unit.

Remove the three screws (1) which hold Case Modem in place. (Figure 3.5)

Remove the two screws (2) which hold the main PCB in place.

Remove the main PCB and power supply PCB from Bottom Cabinet.

**NOTE:** When removing the main PCB from Bottom Cabinet, there is a knob that needs to be moved a little to the left to make room.

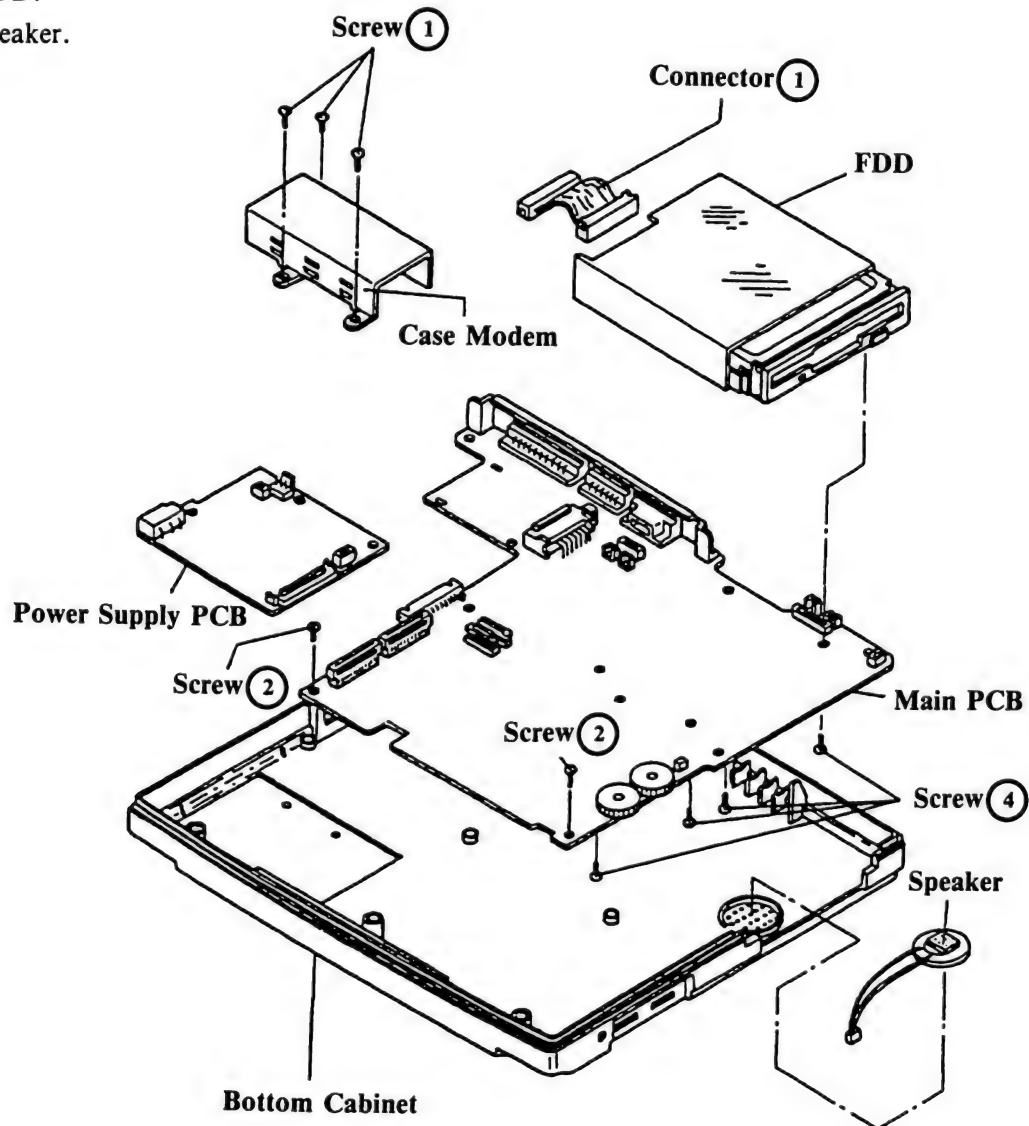
Pull the main PCB and power supply PCB apart.

Remove the four screws (4) which hold the main PCB and FDD in place.

Unplug connector (1) from the main PCB and FDD.

Remove the FDD.

Remove the speaker.



**Figure 3.5**

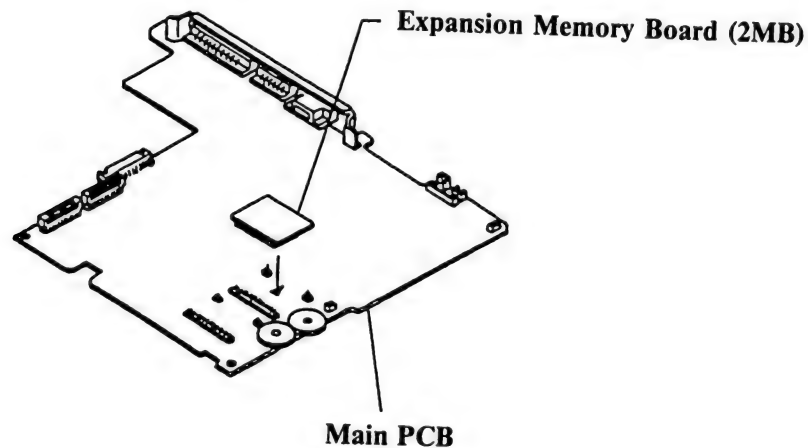
**DISASSEMBLY INSTRUCTIONS FOR C286-LT (Continued)**

**3.6 MEMORY PCB (OPTION) INSTALLATION**

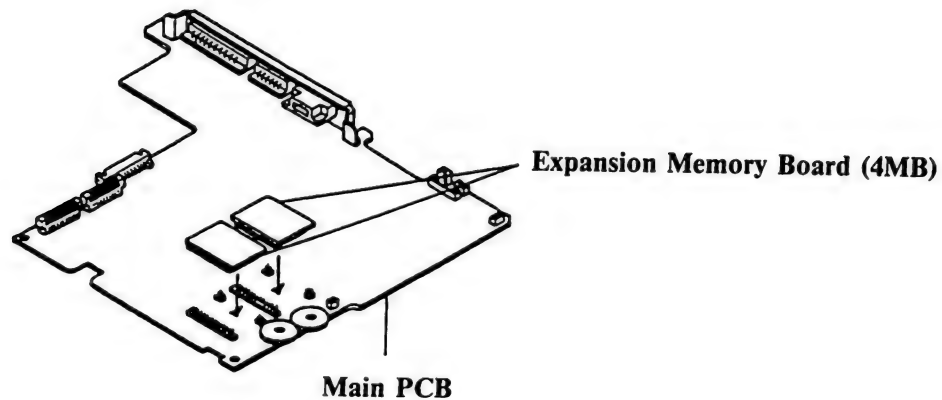
Follow the instructions under 3.1 to remove the keyboard.

Install the memory PCB in locations CN23, CN25 and CN26 on the main PCB (2 MB version). (Figure 3.6)

Install the memory PCB in locations CN23, CN25 and CN26 and CN24, CN27 and CN28 on the main PCB (4MB version). (Figure 3.7)



**Figure 3.6**



**Figure 3.7**

### 3.8 TROUBLESHOOTING ERROR MESSAGES

#### TROUBLESHOOTING GUIDE

Error Messages	Customer Response	Service POD Test (H)
1. DMA 1 error	See your dealer	Test 0B
2. DMA 2 error	See your dealer	Test 0C
3. Interrupt controller 1 error	See your dealer	Test 0D
4. Interrupt controller 2 error	See your dealer	Test 0E
5. PIO error	See your dealer	Test 0F
6. Parity error	See your dealer	Test 10
7. Real time clock is not working	See your dealer	Test 1E
8. Illegal shutdown code in CMOS	See your dealer	Test 02
9. Virtual Mode CPU error	See your dealer	Test 26
10. Parity error on main circuit board	See your dealer	Misc
11. Parity error on expansion bus	See your dealer	Misc
12. Non-recoverable error-Processor halted	See your dealer	Misc
13. Press F1 key to continue	Press F1 key	Misc
14. Battery Failure	Run Setup Utility/See your dealer	Test 11
15. Base memory configuration error	Run Setup Utility	Test 17
16. Extended memory configuration error	Run Setup Utility	Test 18
17. Floppy 0 configuration error	Run Setup Utility	Test 1A
18. Floppy 1 configuration error	Run Setup Utility	Test 1A
19. Coprocessor (80287) configuration error	Run Setup Utility	Test 1D
20. The realtime clock has not been initialized	Run Setup Utility	Test 1E
21. Keyboard	Check keyboard	Test 14
22. Key switch is off. Turn it on to continue	Turn keylock on	
23. Boot failure, check disk and hit any key to try again	Check for non-MS-DOS disk in Drive A;; run Setup Utility	Misc

#### PLEASE NOTE

THE FOLLOWING OVERVIEW OF POWER ON DIAGNOSTICS TESTS IS FOR INFORMATION ONLY. COMPONENT LEVEL REPAIRS TO THE C286-LT PCB ARE NOT AUTHORIZED BY COMMODORE. SEE PCB REPLACEMENT PROCEDURES IN THIS SECTION.

### 3.9 POWER ON DIAGNOSTICS

#### **C286-LT Troubleshooting**

The Commodore 80286 ROM bios contains a "Power on Diagnostic" program which tests the functions of hardware and checks the configuration prior to passing control to the operating system.

The number of the test routine being run is passed to addr 03 78 (H) prior to the start of each test section.

The 80286 processor is initialized by the "RESET" signal. Refer to RESET description in IC pinout section, note that "VCC" and "CLK" to CPU must be correct and "HOLD" must not be active for 34 ticks from leading edge to trailing edge of initial reset.

RESET will terminate all instruction execution and local bus activity until it is negated. Prior to fetching, decoding and executing, the first instruction, located at physical address FF FF F0 (H), the 80286, in real address mode, processes some micro code located in its internal ROM, this takes about 38 ticks.

#### **Test 01 (H) 0000 0001 (B)**

The first test performed by the power on diagnostic checks the 8088 flags, the arithmetic logical unit, and the CPU registers.

If a failure is detected in Test 01, a "HALT" instruction is executed. This will stop program execution and prevent the CPU from using the local bus. The 80286 can be forced out of the halted state by "RESET", "NMI" or "INTR" (when "INTR" is used for RESTART, the interrupt enable bit of flag register must be on (set to 1), and the effective address computed from CS:IP will point to the next instruction after the halt instruction).

\*\*\*Failure in test 01 indicates defective 80286.

#### **Test 02 (H) 0000 0010 (B)**

This routine checks to see if a "SHUTDOWN" has occurred. A shutdown can indicate a severe error which would prevent the CPU from further processing.

**NOTE:** A halt or shutdown condition is signaled externally, by the 80286 as a bus operation. Low states on S0', S1', COD/INTA', and a high state on M/IO' indicate a halt or shutdown. The state of address line 1 will indicate which condition, A1 high is halt, A1 low is shutdown.

After the test number is moved to the parallel port a check for keyboard reset is conducted and the program branches to test 04 (H) if it has.

The check for shutdown begins by examining the 8242 keyboard controller status port. In all ten shutdown conditions are tested, of these, three unexpected shutdown conditions, numbers 6, 7 or 8, any one of which if true, will generate the console message:

"Illegal Shutdown Code in CMOS"

**NOTE:** Branch information for shutdown routines are stored in CMOS memory. The shutdown command is sent to the 8242, the UPI status port, which will halt the CPU. Return depends on the shutdown code in CMOS memory.

An error code, F6, F7 or F8, (HEX) is sent to the parallel port before calling the display routine which generates the above message.

In real address mode a shutdown could occur under the following conditions:

Interrupt number 8, interrupt number 13, or a "CALL INT" or "PUSH" instruction which wraps stack segment when SP is ODD.

Routines also perform valid shutdowns to exit protected mode. During these the DMA page register will be initialized and interrupt control words (ICW) 1, 2, 3 and 4 will be reinitialized. Other routines within the test enable "NMI", parity and set the I/O check bit.

\*\*\*Failures in test 02 could indicate problems on the local bus, or expansion bus. This would include: 80286, OTI-051, OTI-053, OTI-052, or any third party cards.

#### **Test 03 (H) 0000 0011 (B)**

Eprom checksum test verifies contents of eprom by adding bytes and checking for result of zero. A compensation byte is factored into the addition to make the sum zero.

Detection of an error results in a halt condition and would invalidate tests 01 and 02.

\*\*\*Failure in test 03 indicates defective ROM.

**Test 04 (H) 0000 0100 (B)**

Test 04 checks the DMA page registers by writing and reading bits starting at address 80 (H).

\*\*\*Failure in test 04 indicates possible defective OTI-053, OTI-052, or local bus.

**Test 05 (H) 0000 0101 (B)**

Timer 1 and timer 2 are checked for correct operation. Interrupts are masked off during the test.

\*\*\*Failure in test 5 indicates possible defective OTI-053, OTI-052.

**Test 06 (H) 0000 0110 (B)**

Memory refresh test. Timer and DMA are setup to initiate refresh cycles every 15.1 microseconds. Size of virtual memory is calculated.

\*\*\*Failure in test 06 indicates possible OTI-053, OTI-052, Refresh logic or memory problem.

**Test 07 (H) 0000 0111 (B)**

Test 07 checks the 8242 keyboard controller by writing and reading the keyboard buffers.

\*\*\*Failure in test 07 indicates possible defective 8242 or associated circuitry.

**Test 08 (H) 0000 1000 (B)**

Test 08 writes and reads the first 128K of RAM and verifies block size is 128K. First pass writes addresses into data, the second pass writes the complement of the address into data. Memory is cleared after test. The battery status is also confirmed in test 08.

\*\*\*Failure in test 08 indicates possible defective RAM or RAM logic.

**Test 09 (H) 0000 1001 (B)**

Test and configure video. A search is made to determine if MDA, CGA or a special video adapter is configured, if not the onboard VGA is enabled and a call to VGA bios is executed. The dip switches are read to determine the default video mode.

**NOTE:** The mode register setting in the GD610 controls the reset signal to the onboard VGA controller chip. If no special video adapters are found on the expansion bus then "NOVID" from the GD610 is negated.

On completion of this test the title and copyright message are displayed.

**Test 0A (H) 0000 1010 (B)**

Test RAM from 128K to 640K. A display message is generated indicating that the base RAM of 128K, Test 08, is OK. Blocks of 128K, starting at 128K are then tested by writing, reading and verifying RAM. The first pass writes addresses to data, that is, the address which defines the physical location is also used as the bit pattern that is being written. The second pass writes complement of address into data.

The test displays results in blocks of 128K to the console each time a 128K boundary is reached.

At completion of the onboard memory test the CPU is placed in virtual mode and a test for virtual memory (over 1 MEG) is started.

**NOTE:** See test 26 (H).

\*\*\*Failure in test 0A indicates a defective RAM.

**Test 0B (H) 0000 1011 (B)**

DMA controller #1 register check.

Four current address registers (16 bits wide, each) and four current word count registers (16 bits wide, each) for each of the four DMA channels are written to and read from to verify operation.

A failure in test 0B will generate the following display on the console:

"DMA 1 error"

The beeper will sound, and a halt instruction will be executed.

\*\*\*Failure in test 0B indicates a defective OTI-053, OTI-052.

**Test 0C (H) 0000 1100 (B)**

DMA controller #2 register check. The second functional 8237 containing four current address registers (16 bits wide, each) and four current word count registers (16 bits wide, each) within the OTI-053, OTI-052 are written to and read from to verify operation.

Successful completion of the test 0C will set the modes for DMA channels 0 through 3 and enable cascading by channels 4, 5 and 6 (DMA 1).

A failure in test 0C will generate the following display on the console:

“DMA 2 error”

The beeper will sound, and a halt instruction will be executed.

\*\*\*Failure in test 0C indicates a defective OTI-053, OTI-052.

**Test 0D (H) 0000 1101 (B)**

Interrupt controller #1 test. Patterns are written to, and read from the interrupt mask register (IMR) which controls the interrupt request register (IRR).

A verification is made that no interrupts can occur if “IMR” is set to FF (H). A vector is initialized to a temporary interrupt service routine in the event of a failure.

A test for correct timer 0 interrupt is also made.

A failure in test 0D will generate the following display on the console:

“Interrupt controller 1 error”

The beeper will sound, and a halt instruction will be executed.

\*\*\*A failure in test 0D indicates a defective OTI-053, OTI-052.

**Test 0E (H) 0000 1110 (B)**

Interrupt controller #2 test. The second functional 8259 contained in the OTI-053, OTI-052 is tested as in test 0D, without timer test.

A failure in test 0E will generate the following display on the console:

“Interrupt controller 2 error”

The beeper will sound, and a halt instruction will be executed.

\*\*\*A failure in test 0E indicates a defective OTI-053, OTI-052.

**Test 0F (H) 0000 1111 (B)**

Check peripheral in/out register. Write and read from PIO register.

A failure in test 0F will generate the following display on the console:

“PIO error”

The beeper will sound, and a halt instruction will be executed.

\*\*\*A failure in test 0F indicates a defective OTI-053, OTI-052.

**Test 10 (H) 0001 0000 (B)**

RAM parity test. Blocks of RAM are written to and read from, parity check for odd parity is made. Parity disabled after successful test.

**NOTE:** C286-LT does not use parity, third parity boards that use parity will enable parity.

“NMI” is enabled and a service routine for a parity error generates the following console message.

“Parity error”

The beeper will sound, and a halt instruction will be executed.

\*\*\*Failure in test 10 indicates a defective RAM, third party card, NMI, or local bus.

**Test 11 (H) 0001 0001 (B)**

Test CMOS clock for battery failure and checksum failure.

Beeper will sound if failure is detected. Console will display:

“Battery failure” or “CMOS checksum failure” or both.

\*\*\*Failure of test 11 indicates a defective battery, or defective oscillator.

**Test 12 (H) 0001 0010 (B)**

This test is disabled. It is used only in manufacturing tests.

The beeper will sound for a set length prior to the start of test 13 (H). In a system which has passed all tests to this point the beeper sound heard now would be the one heard in the power up routine.

**Test 13 (H) 0001 0011 (B)**

Setup interrupt controller and move vector tables to RAM. Vector addresses are fetched from top 8K module.

**NOTE:** Vectors for video were setup in test 09.

Master and slave interrupts are enabled at this point.

Test 13 does not create any error messages.

**Test 14 (H) 0001 0100 (B)**

Keyboard test. Functional test of the 8242 keyboard controller at U203. A test for a stuck key on keyboard is performed. Check is made to see if key lock is locked.

A failure in test 14 will display the following error message on console:

“Keyboard error”

\*\*\*Error indicates a defective 8242 controller or a defective keyboard.

**Test 15 (H) 0001 0101 (B)**

Test and configure the parallel port. Parallel port addresses are setup, reads and writes to ports are done. Set time out. No error messages are generated by this test.

**Test 16 (H) 0001 0110 (B)**

Configure serial COM1 and COM2 for OTI-052. Read serial interrupt ID, set number of serial channels.

No error messages are generated by this test.

**Test 17 (H) 0001 0111 (B)**

Configure memory less than 640K. Parity (for EXPANSION RAM) is enabled.

Memory was tested in test 0A, and “CMOS STATUS” set. A check for a warm boot (ALT/CNTRL/DEL) is made and a comparison of the old and new memory configuration is performed. If a memory size mismatch is detected, the beeper will sound and the following non-fatal error message will be displayed on the console:

“Base memory configuration error”

The new configuration is stored.

\*\*\*Check the settings for RAM size in the setup utility if you encounter this message.

**Test 18 (H) 0001 1000 (B)**

Configure memory over 1 megabyte (virtual memory). Check is made on address line 20, a low indicates virtual address mode.

CMOS status is checked as in test 17, a memory size mismatch will sound the beeper and generate the following non-fatal error message on the console:

“Extended memory configuration error”

The new configuration is stored.

\*\*\*Check the settings for RAM size in the setup utility if you encounter this message.

**Test 19 (H) 0001 1001 (B)**

Configure keyboard test. Setup keyboard buffers, enable keyboard interrupt and test if key switch is turned to the on position.

If the key switch is off the following message will be displayed on the console:

“Key switch is off. Turn it on to continue.”

**NOTE:** You are in a loop until you turn on the key switch.



**Test 1A (H) 0001 1010 (B)**

Configure the floppy disk drive. Calculate number of floppy drives present. Check drive type, compare settings stored in CMOS, if a mismatch the following message will be displayed on console:

“Floppy 0 configuration error”

\*\*\*Check settings in setup utility if above message is displayed.

Test checks second floppy configuration, if a mismatch the following message will be displayed on the console:

“Floppy 1 configuration error”

\*\*\*Check settings in setup utility if above message is displayed.

New configuration is stored in CMOS. Floppy interrupt is enabled.

**Test 1B (H) 0001 1011 (B)**

Configure the hard drive. Check configuration if a mismatch hard drive will not be setup.

No error message is generated.

**Test 1C (H) 0001 1100 (B)**

Test number is not moved to parallel port for this configuration. This routine only turns on the game card bit in the “EQUIP FLAG”.

No error message is generated.

**Test 1D (H) 0001 1101 (B) — Not valid C286LT**

Configure 80287 coprocessor. Check if 80287 is present. Enable 80287 interrupt and set “EQUIP FLAG” if it is. Compare configuration with CMOS, store new configuration, beep the speaker, and display the following message is setup changed.

“-- Coprocessor (80287) configuration error”

\*\*\*Check setup utility for correct settings if this message is displayed.

**Test 1E (H) 0001 1110 (B)**

Check CMOS clock to see if it was initialized and is working. Enable timer interrupt. Sound beeper, and initialize if failure detected, then display one of the following messages on the console:

“-- The Real Time Clock has not been initialized”

OR: “-- Real Time Clock error”

\*\*\*Check the OTI-054 if second message above is displayed.

**Test 1F (H) 0001 1111 (B)**

Generate a new CMS checksum and save it in CMOS RAM. Call made to auto configuration program at this point.

No error message generated.

**Test 20 (H) Not Implemented**

**Test 21 (H) 0010 0001 (B)**

Initialize ROM drivers, including hard drive. Checksum generated, and all ROMS tested.

System will now begin boot up.

System speed is determined, 6 MHz, 8MHz or 12MHz.

\*\*\*Refer to operations manual for opening screen display.

**Tests 22, 23 Not Implemented**



## 3.7 WIRING DIAGRAM

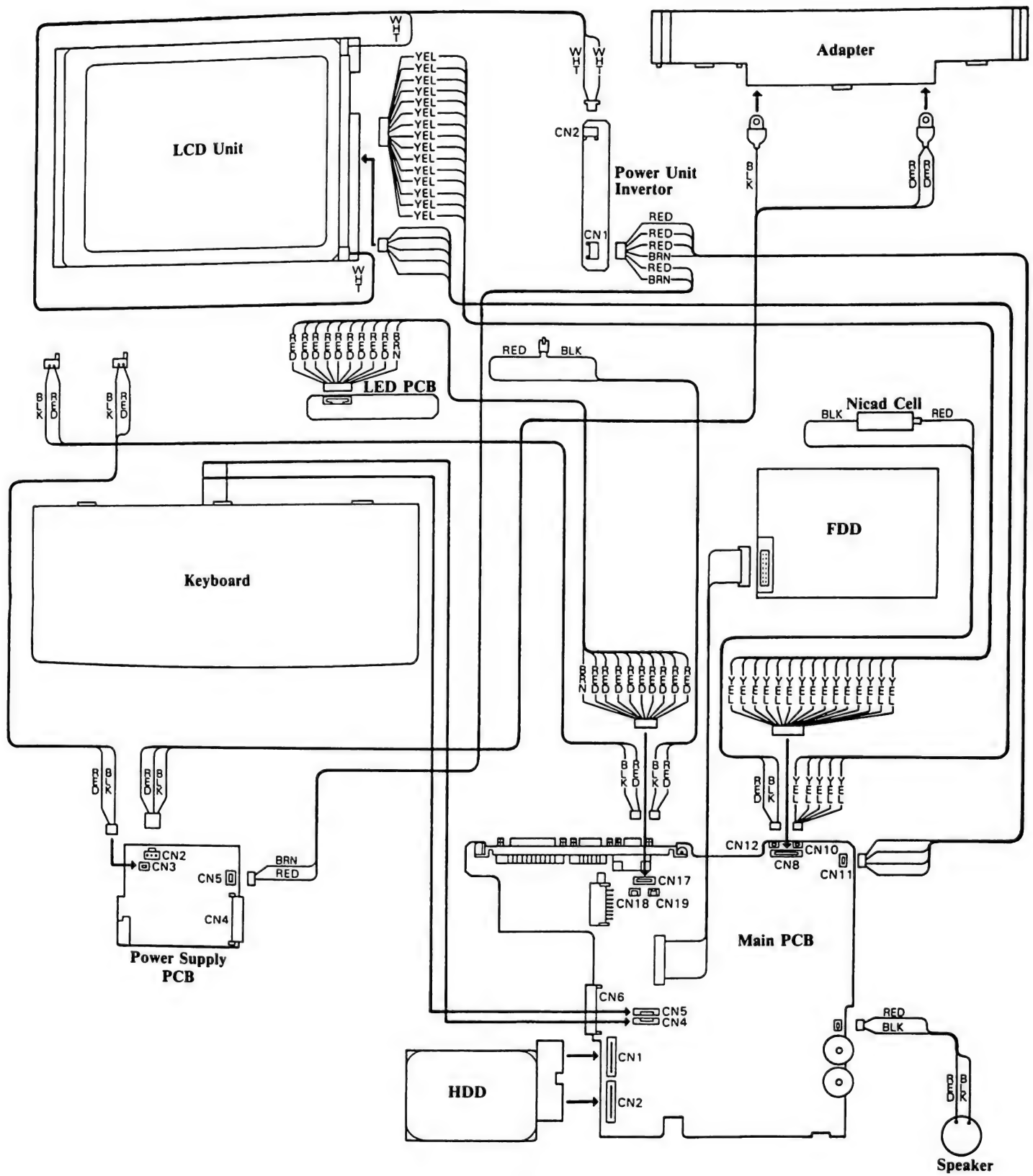


Figure 3.8

**Test 24 (H) 0010 0100 (B)**

Test operation of the RTC chip. Recheck battery, make sure clock is counting, test memory.  
System will execute a halt instruction on memory failure. No error message is generated.

**Test 25 (H) 0010 0101 (B)**

Used in manufacturing to loop through diagnostics.

**Test 26 (H) 0010 0110 (B)**

Virtual memory test (over 1 megabyte). Call made to this routine from test 09.

Display Message: "Testing Extended RAM"

Display Message: "Total System RAM = XXXX" at finish.

During this test the exception interrupt vector tables and descriptor tables are built, and moved from ROM to RAM.

A test of address line 20 is made (controls real or virtual CPU mode). If not in virtual mode display following message:

"Test — 26: Virtual Mode CPU error"

And send F3 (H) (1111 0011 to parallel port. Then execute a halt instruction.

Test address lines 19 through 23 are tested. Shutdown if error. Exception interrupt codes are moved to the parallel port prior to shutdown. The following list defines the code sent to the port and the type of exception interrupt ( EXECPT INT ).

81	(H)	EXECPT INT 01	Single Step
82	(H)	EXECPT INT 02	NMI
83	(H)	EXECPT INT 03	Breakpoint
84	(H)	EXECPT INT 04	Into Detect
85	(H)	EXECPT INT 05	Boundary
86	(H)	EXECPT INT 06	Invalid OP Code
87	(H)	EXECPT INT 07	—
88	(H)	EXECPT INT 08	Double Exception
89	(H)	EXECPT INT 09	Processor Segment Error
8A	(H)	EXECPT INT 10	—
8B	(H)	EXECPT INT 11	Segment Not Present
8C	(H)	EXECPT INT 12	Stack Segment Not Present
8D	(H)	EXECPT INT 13	General Protection Error
8E	(H)	EXECPT INT 14	—
8F	(H)	EXECPT INT 15	—
90	(H)	EXECPT INT 16	Processor Extension Error

Power on diagnostic program is finished at the time of boot up ( end of test 21 ).

Note that during execution of "POD" calls are made to auto configure and to miscellaneous interrupt routines.

All error messages listed in appendix L of operations guide are listed in the overview above with the exception of the following which are generated from the miscellaneous interrupt routines.

10 "Parity error on main circuit board"

11 "Parity error on expansion bus"

12 "Non-recoverable error - Processor halted"

13 "Press F1 key to continue"

Messages 10, 11 are generated after a parity error has been detected and a memory check has determined that it was on the main board, or the expansion bus. If the check finds the error the CPU is halted and message 12 is displayed. If no error is found after the check, message 13 is displayed and processing will continue.

## **SECTION 4**

### **PARTS**

**COMMODORE STOCKED PARTS**  
**C286-LT MAJOR ASSEMBLIES — FIELD REPLACEMENT UNITS (FRU)**

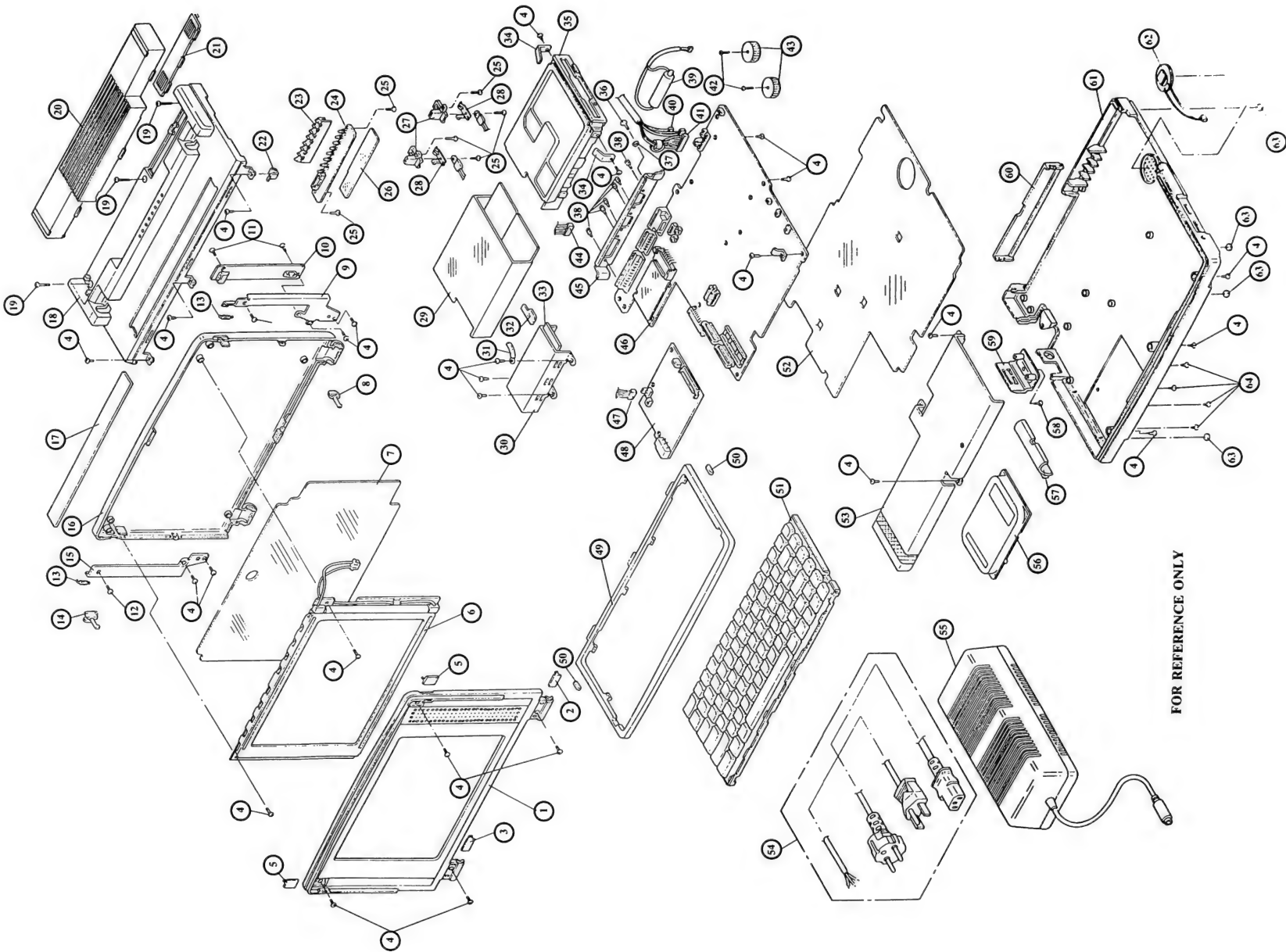
390774-01	AC Power Adapter
903508-15	Power Cord, Shielded
390790-01	Battery Pack
312569-01	Carrying Bag
390840-01	Door — Rear Panel
390839-01	Bezel — Modem (Cover)
363559-01	LCD Display Assembly
363554-01	Keyboard Assembly
390841-01	Lithium Cell
363553-01	PCB Assembly — Power SR170
400500-01*	PCB Main Assembly
312897-01	Drive Assembly — 3.5 Floppy
390843-01	Cable — Floppy Drive
312896-01	Drive Assembly — 20MB Hard Drive
394018-01	Cable — Hard Drive
315984-01	Software Sub Assembly
363573-01**	Manual, Operations Guide

\*Number silk screened on PCB is not the Commodore part number for spare part.

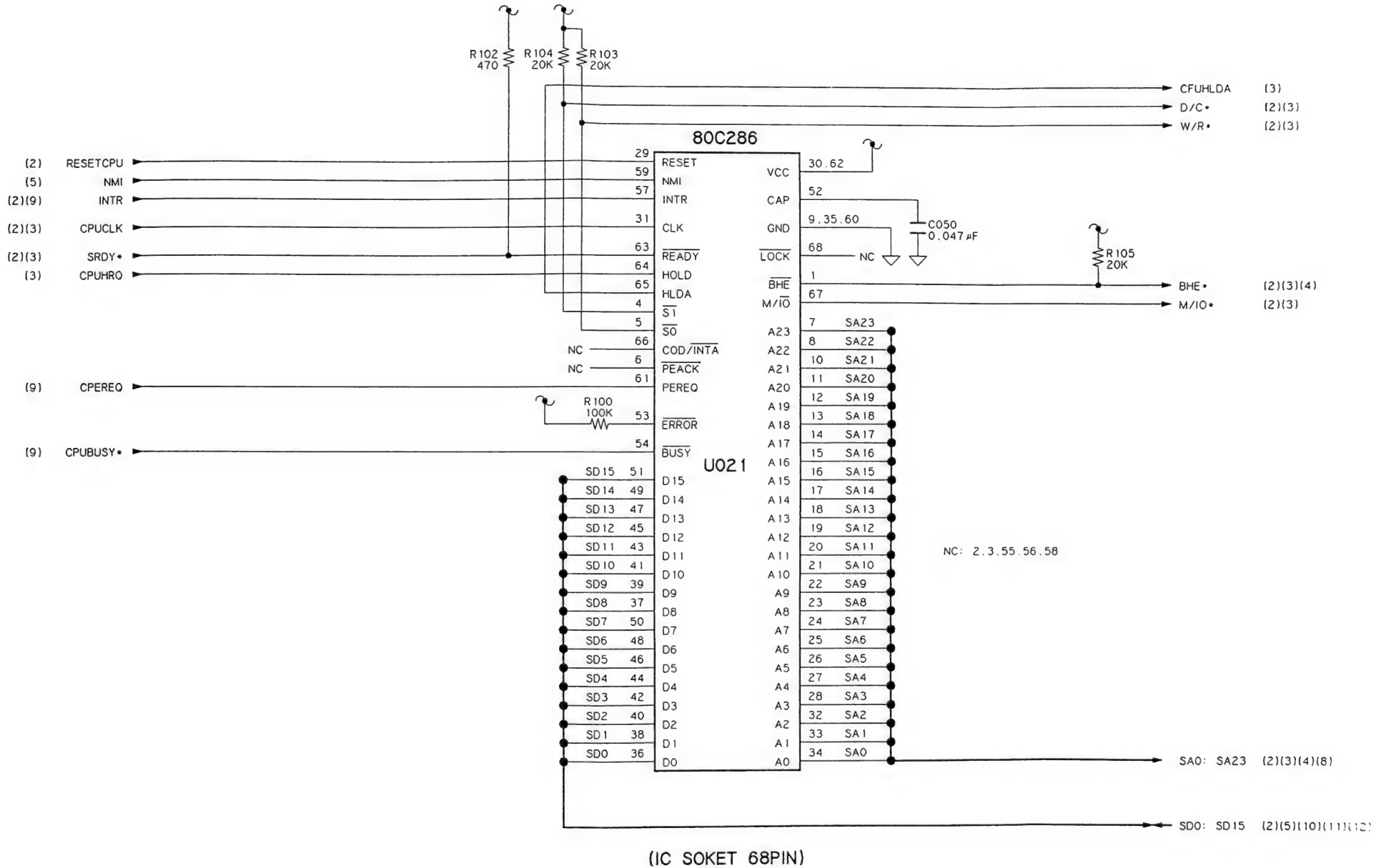
\*\*Operations guide is included in software sub assembly.

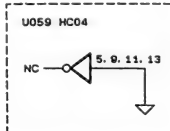
SERVICE REFERENCE PARTS DIAGRAM

DESCRIPTION	REF. #	DESCRIPTION	REF. #	DESCRIPTION	REF. #
Mask LCD	1	Function Sheet	17	Insulator Case Modem	33
Cover Screw Hinge Right	2	Top Cabinet Rear	18	Plate Spring	34
Cover Screw Hinge Left	3	SCR Bin 3x25 (x3)	19	Floppy Disk Drive	35
SCR Bin 3x6 (x26)	4	Nicad Cell 10KR-1700AE-C	20	SCR Bin 4x6	36
Cover Screw LCD (x2)	5	Cover Assy. (Battery)	21	Washer Out TW 4	37
LCD LCM-5630	6	Plate Spring	22	Screw Holder-PFB (x6)	38
Insulator LCD	7	Glass LED	23	Lithium Cell MBC1	39
Stopper LCD Right	8	Pw Board Assy Note LED C1	24	Connecting Cable LCD-PS	40
Bracket LCD Right	9	SCR S-TPG BRZ 2.6x12 (x6)	25	Connecting Cable LCD-SIG	41
Power Unit Inverter	10	Insulator LED PCB	26	SCR Pan Head 1.4x4 (x2)	42
SCR Bin 2.6x5 (x2)	11	Holder Contact (x2)	27	Knob Volume (x2)	43
SCR S-TPG Bin 3x8 (x2)	12	Contact (x2)	28	Connecting Cable LED	44
Extension Spring (x2)	13	Insulator FDD	29	Rear Panel	45
Stopper LCD Left	14	Case Modem	30	Pw Board Assy Note Main	46
Bracket LCD Left	15	Cable Clamp-LBA	31	Connecting Cable Assy 3P	47
Cabinet LCD	16	Insulator Contact	32	Pw Board Assy SR170	48
				Top Cabinet Front	49
				Damper LCD (x2)	50
				Keyboard	51
				Insulator PCB	52
				Shield HDD	53
				AC Cord-Pea	54
				AC Adaptor/Quick Charger	55
				Hard Disk Drive	56
				Connecting Cable HDD	57
				SCR Bin 3x6	58
				Bezel Modem	59
				Door	60
				Bottom Cabinet	61
				Speaker TS30R-8B3A-B	62
				Foot (x4)	63
				Special Screw (x4)	64

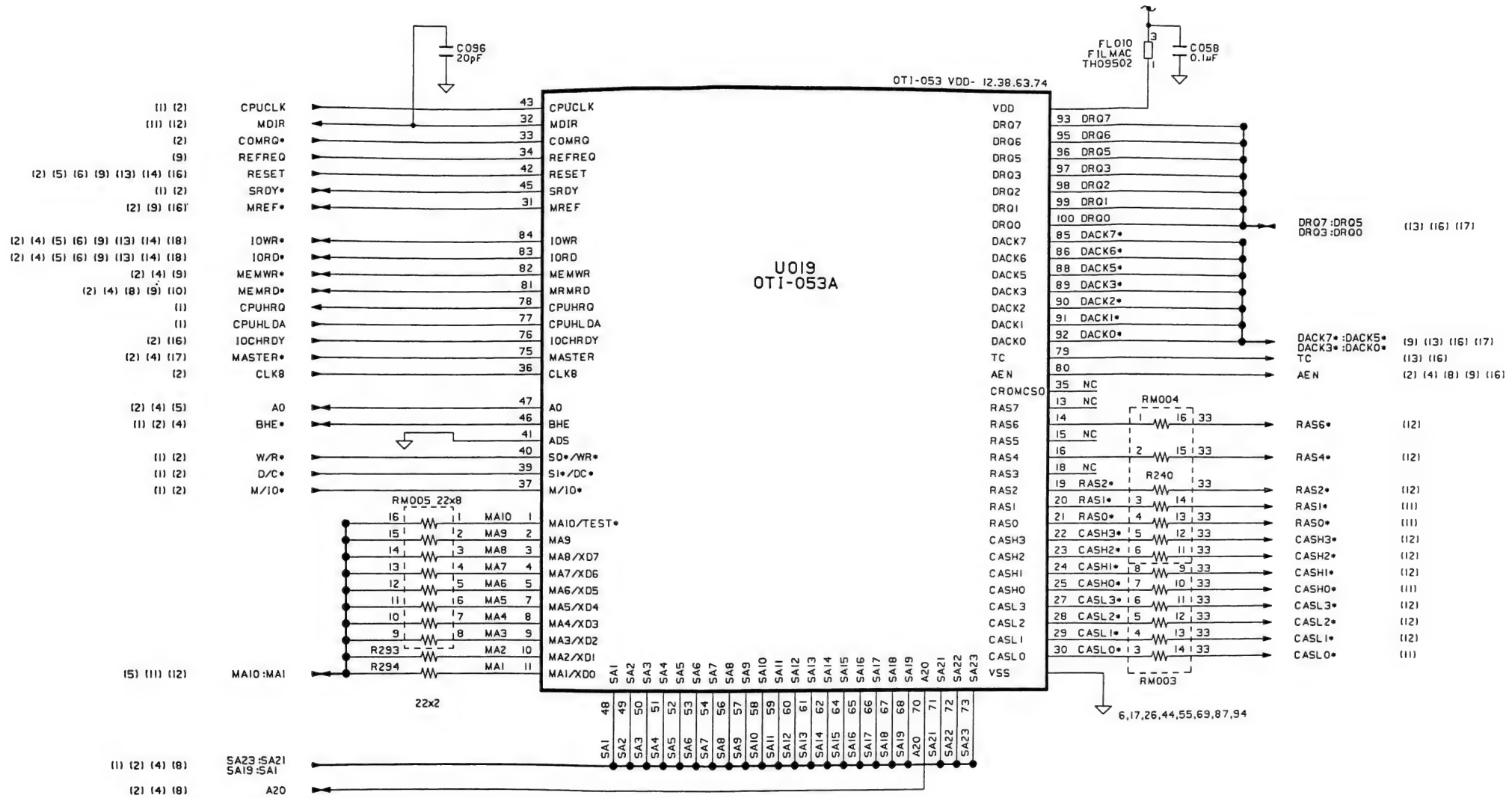


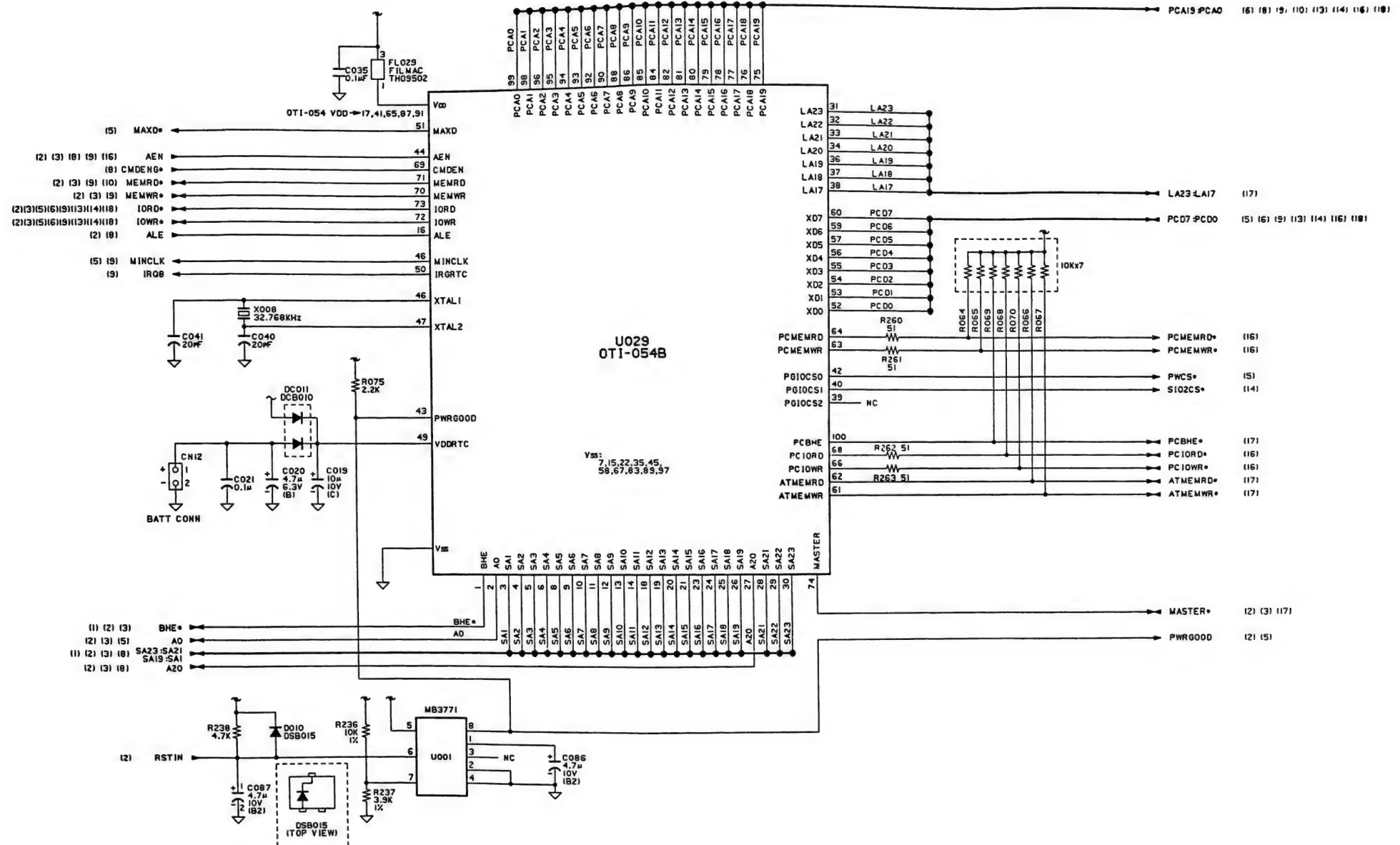
**SECTION 5**  
**SCHEMATICS**

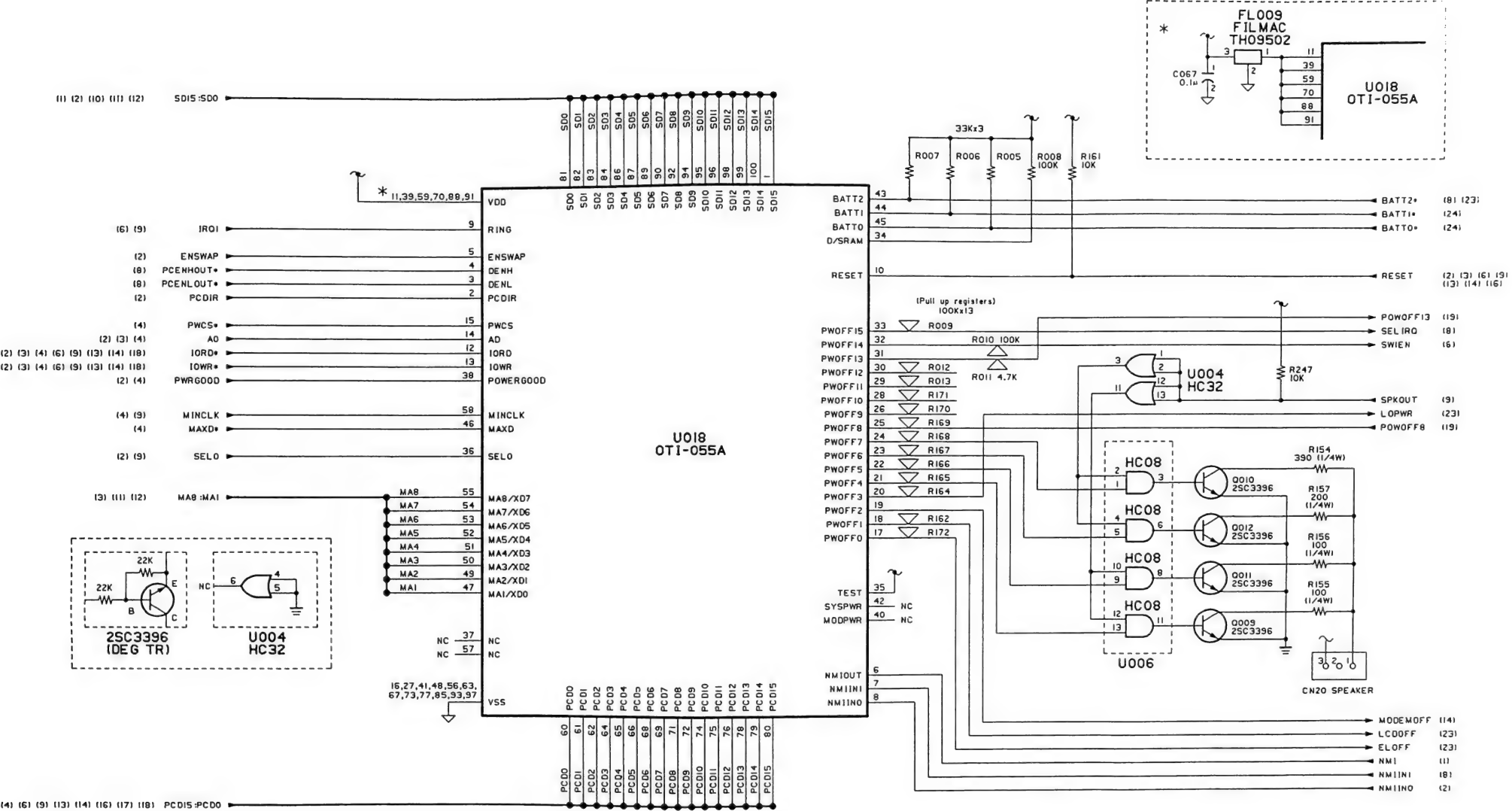


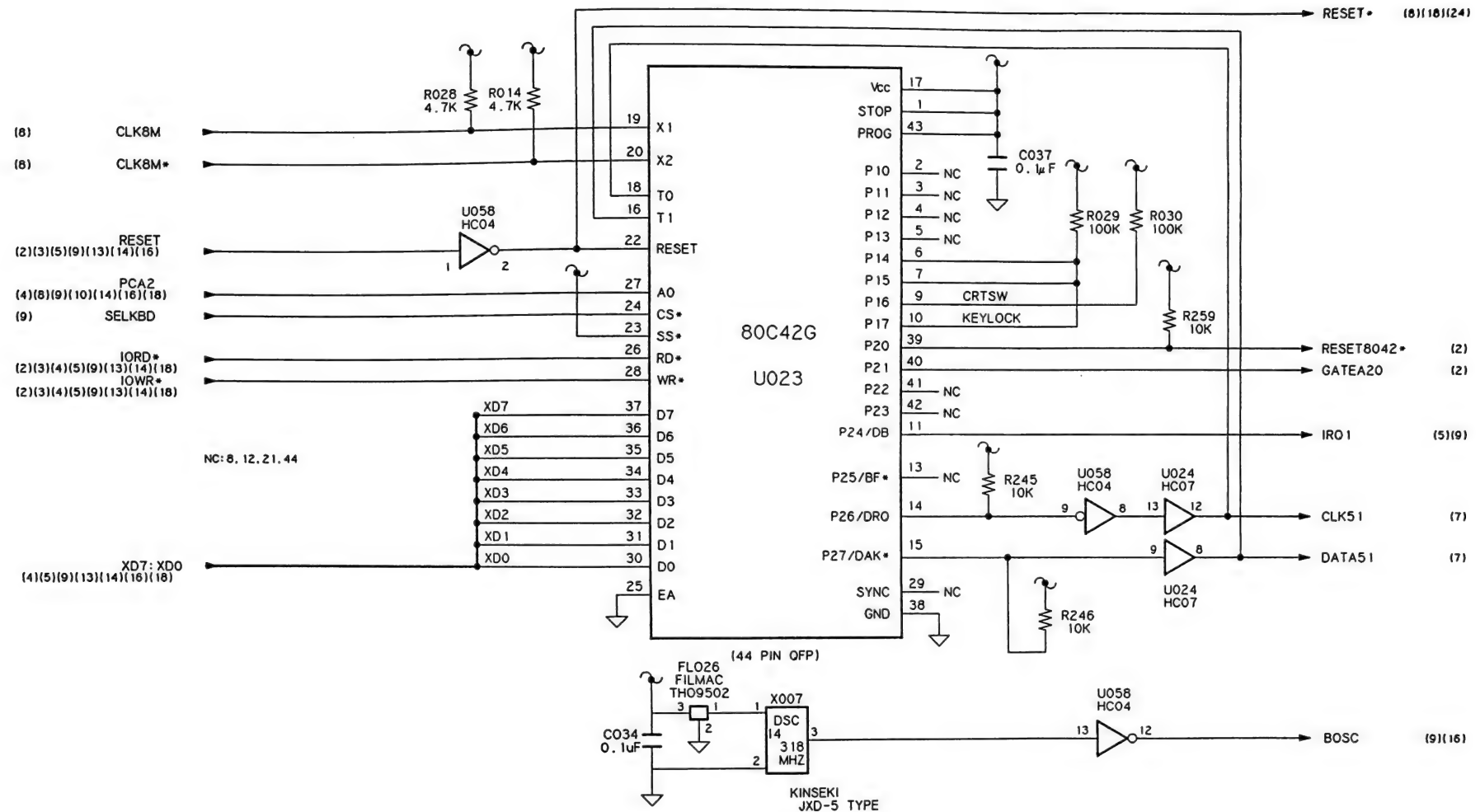


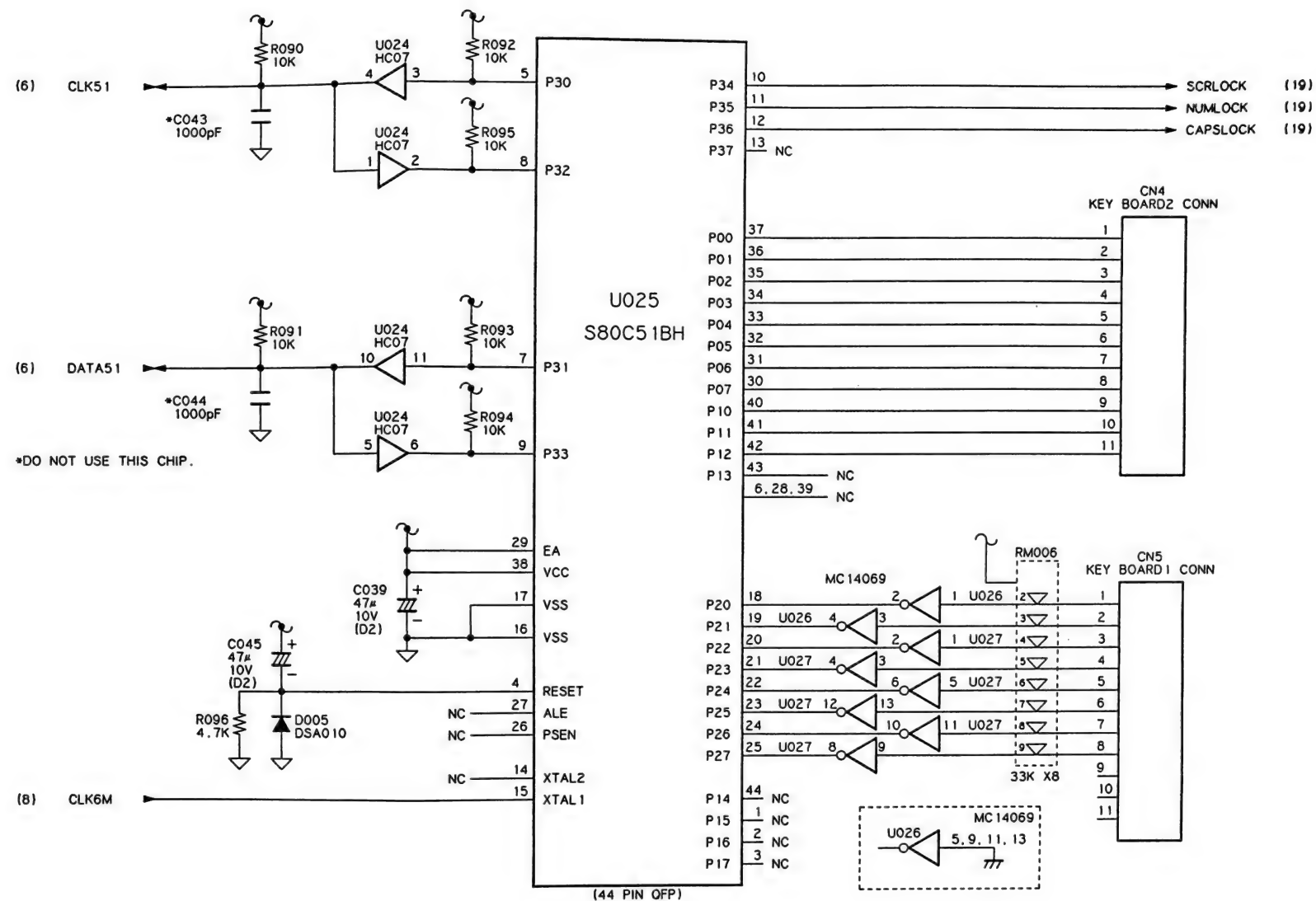


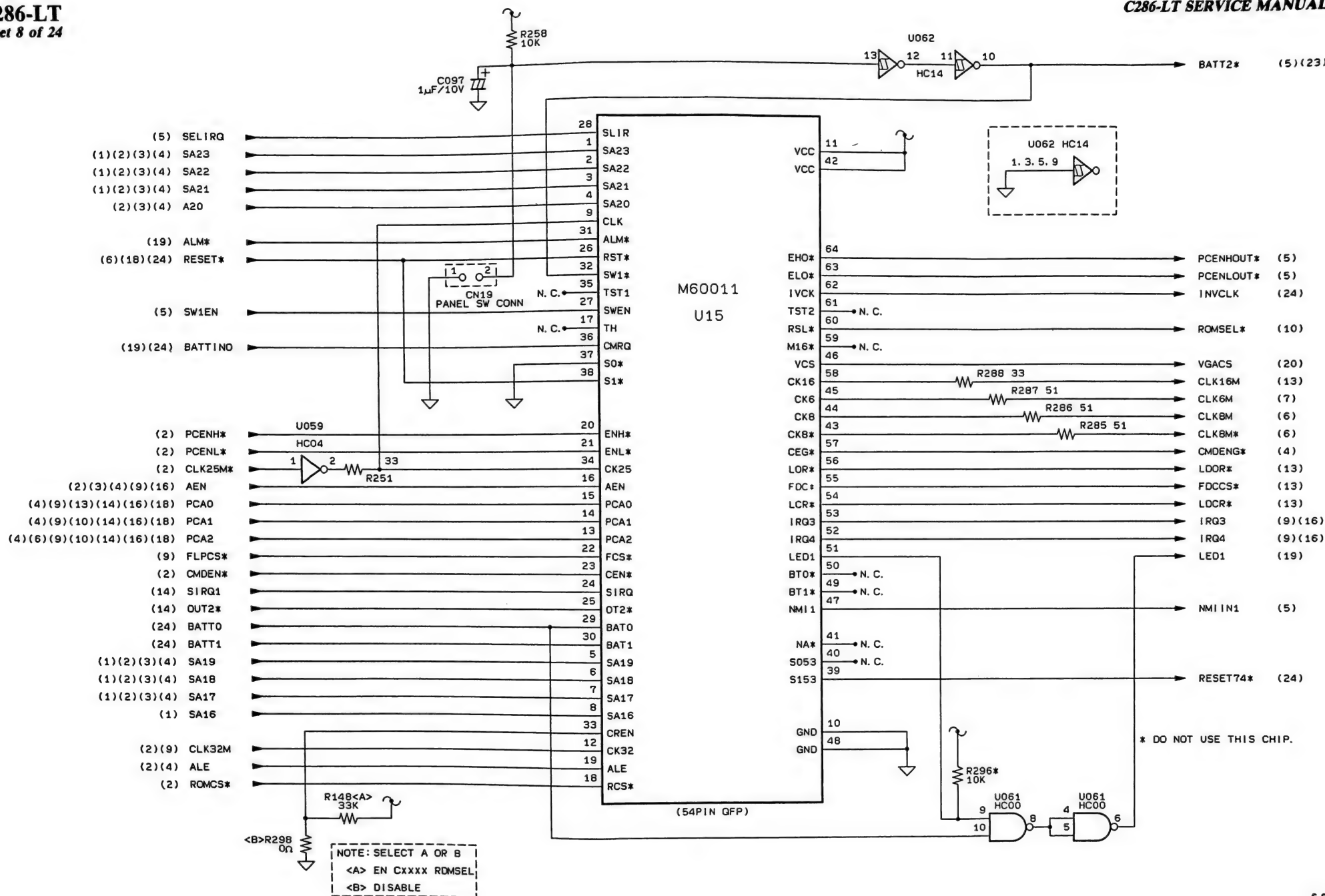


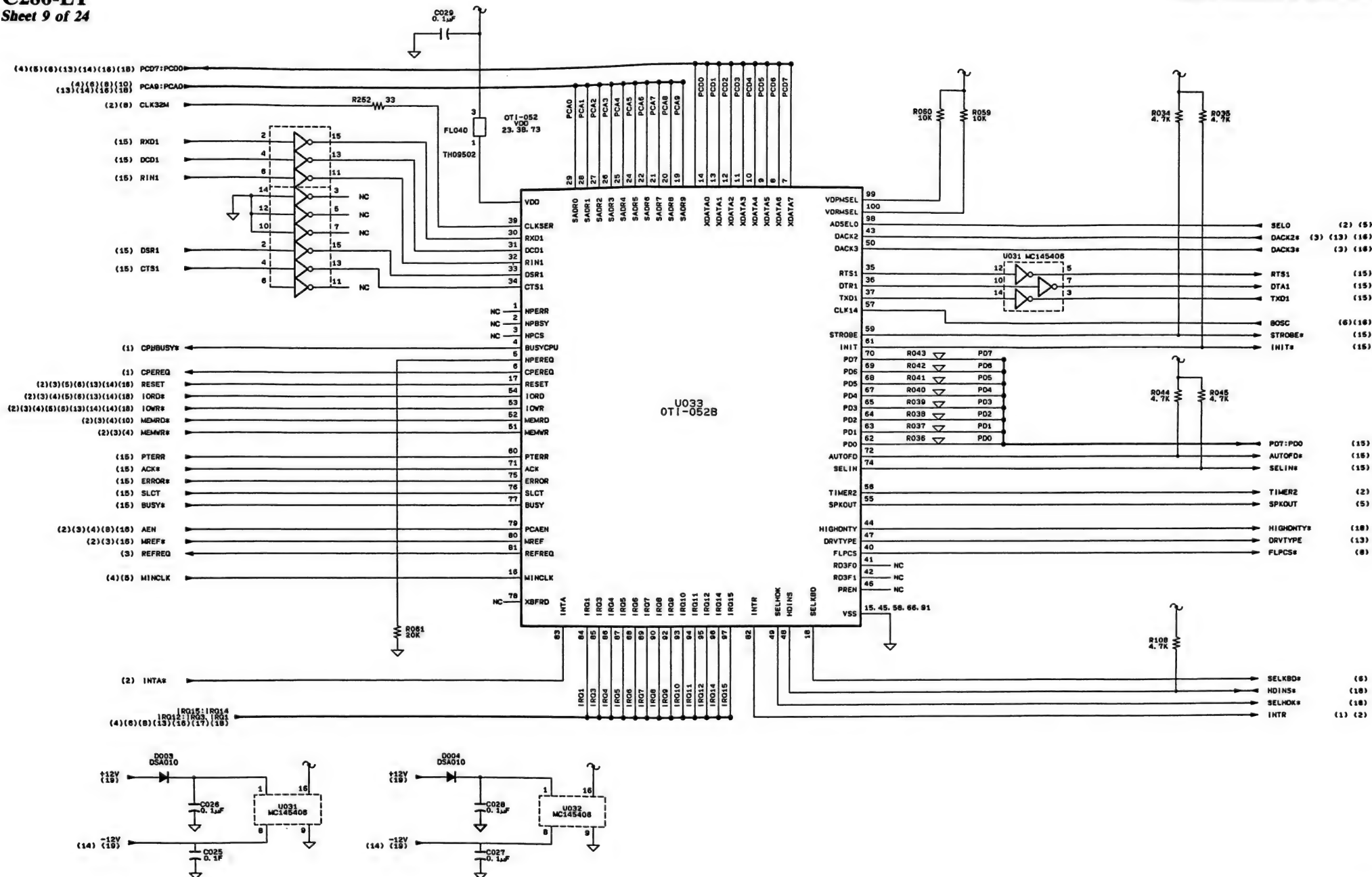


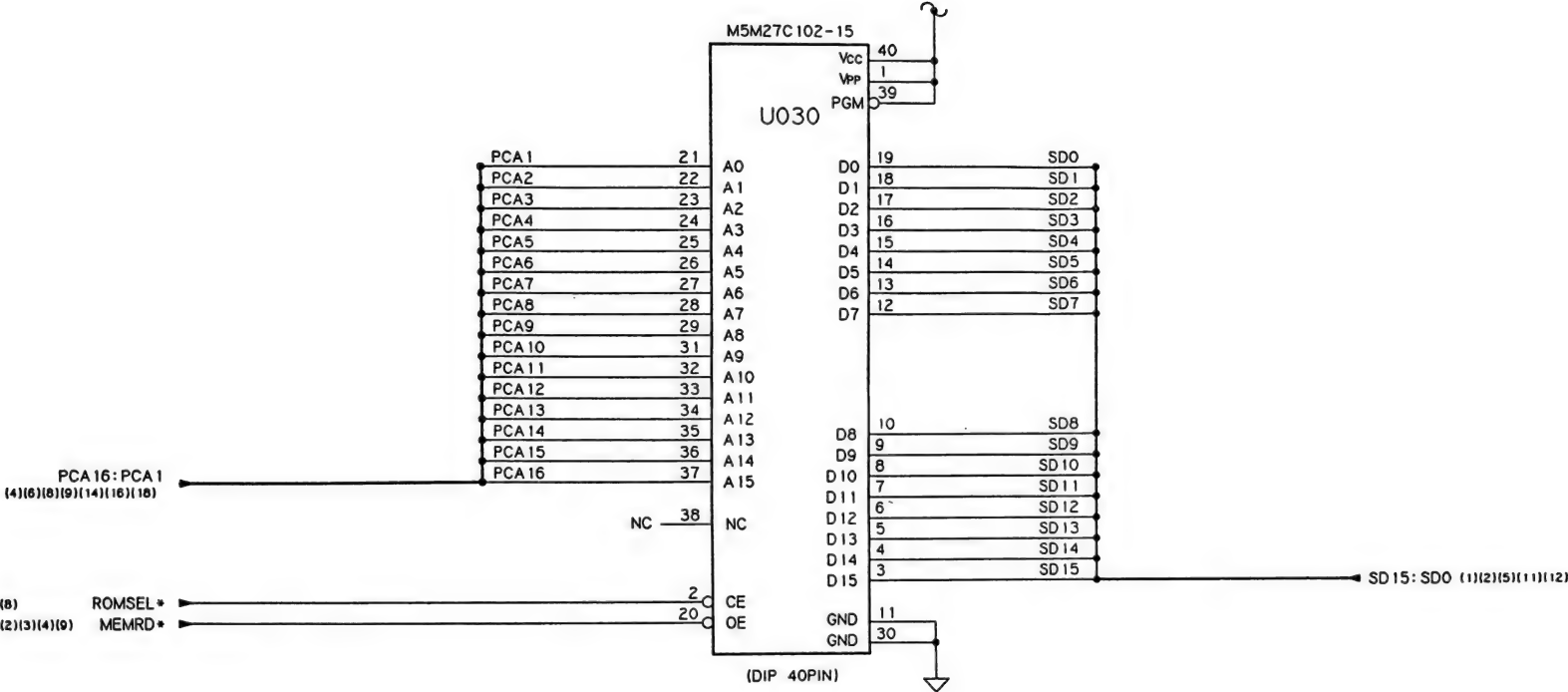




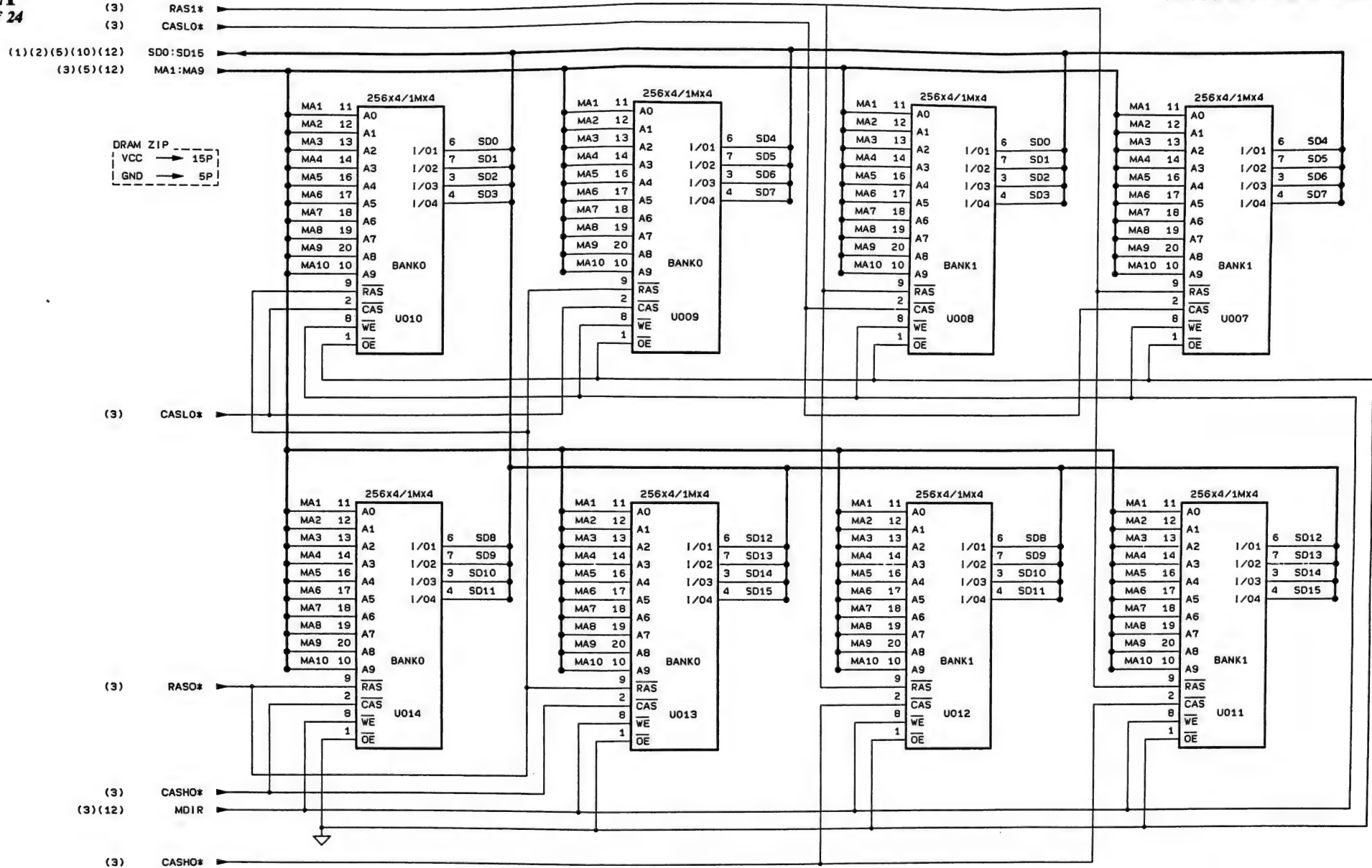






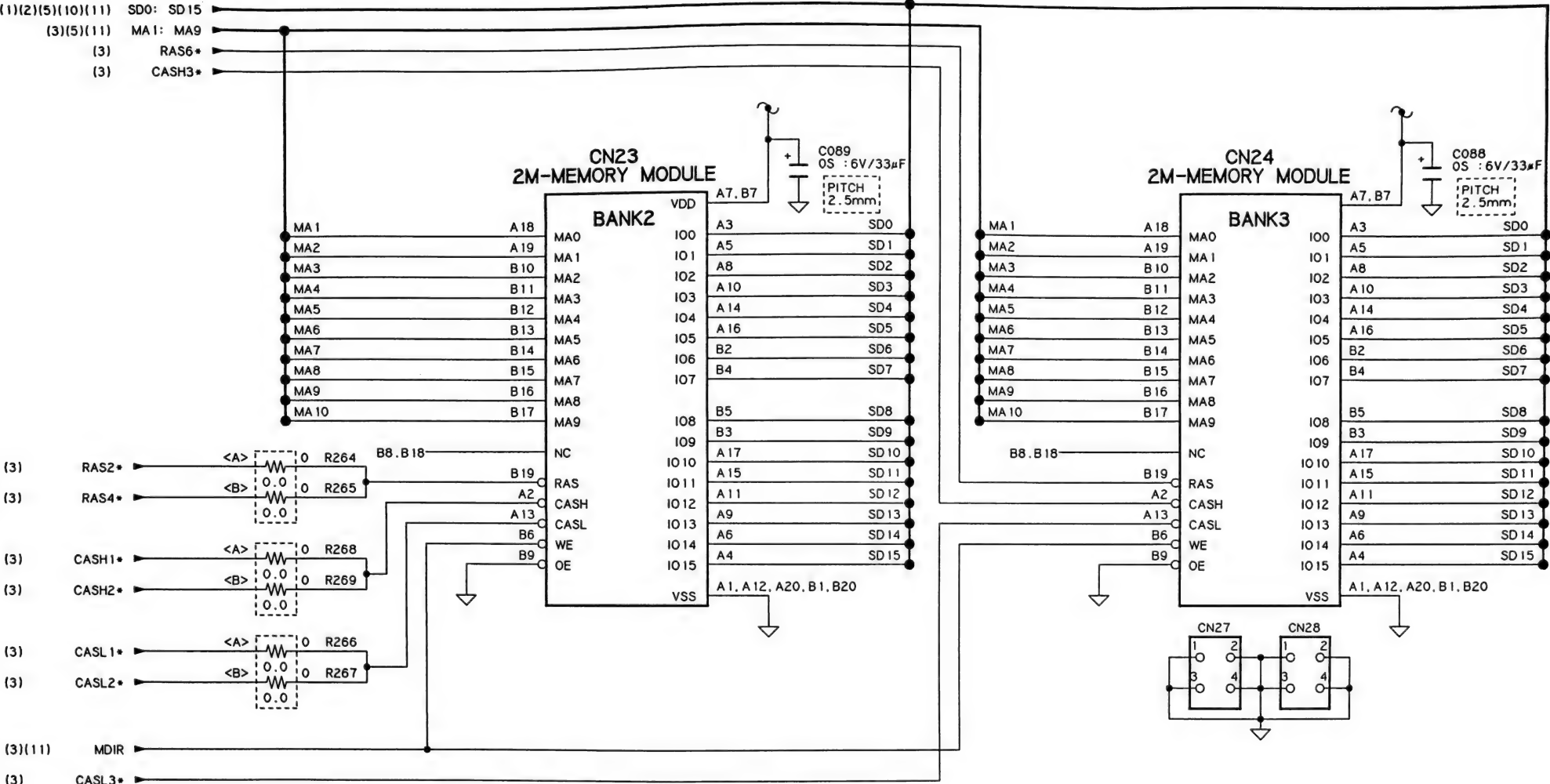


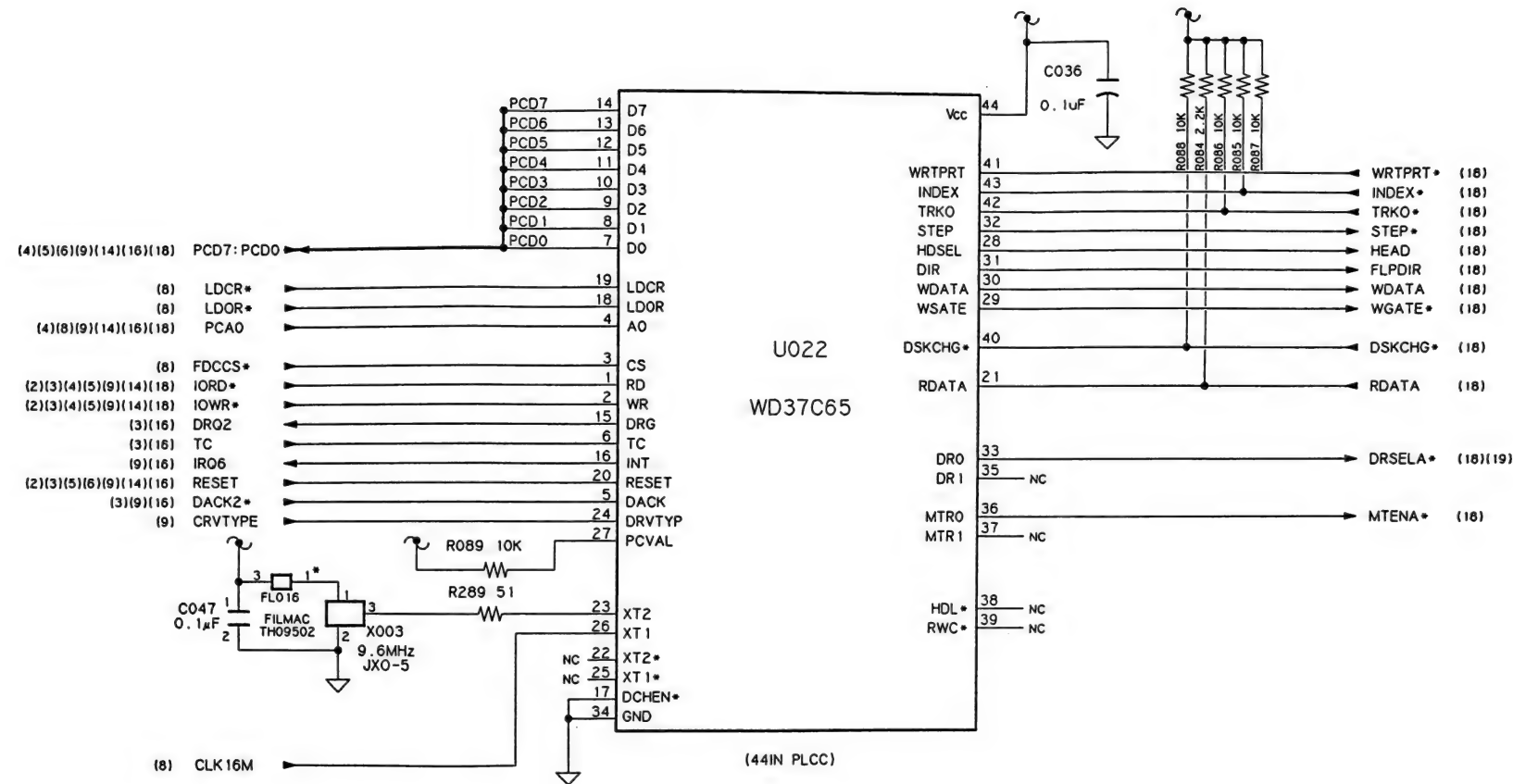


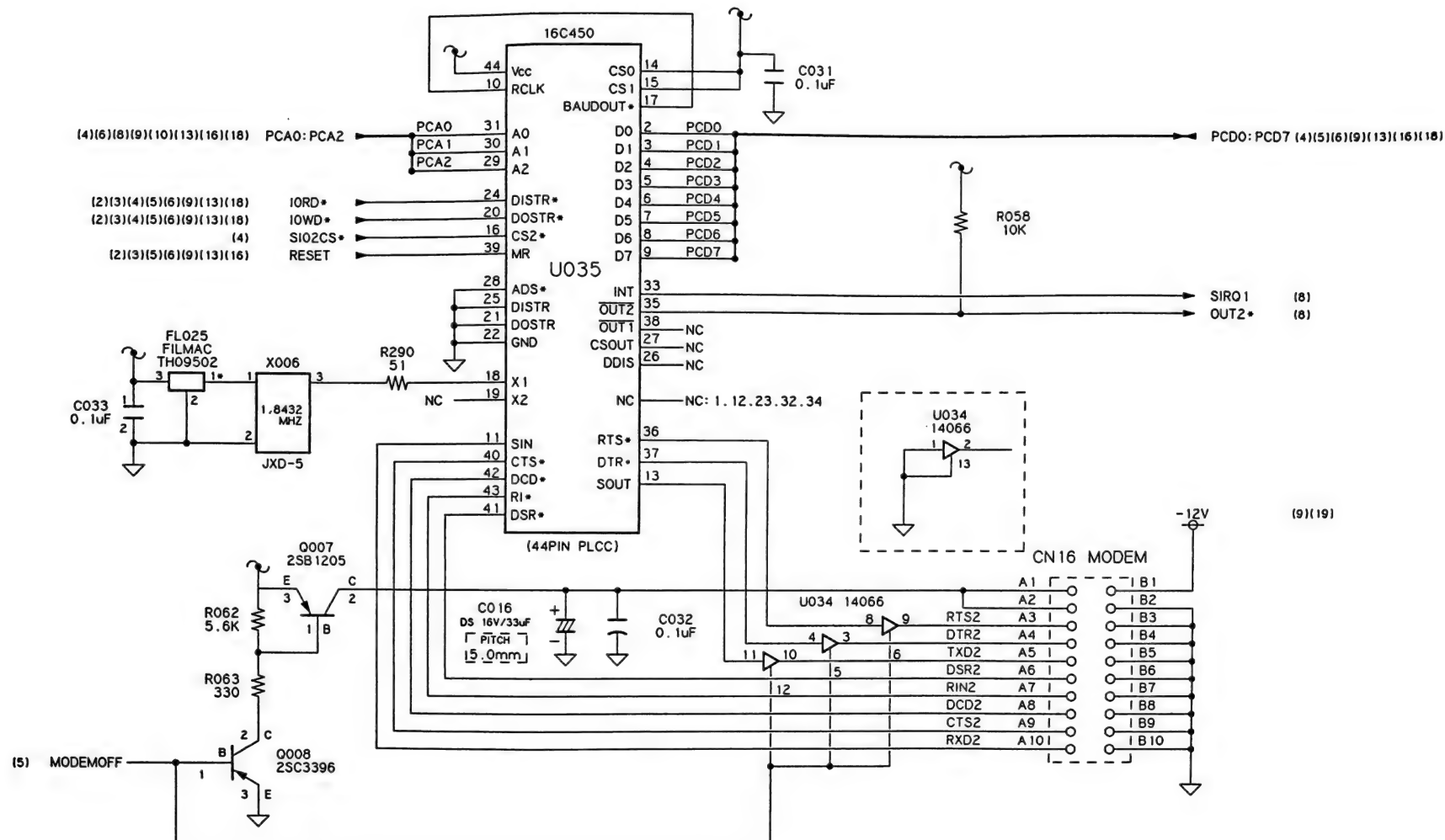


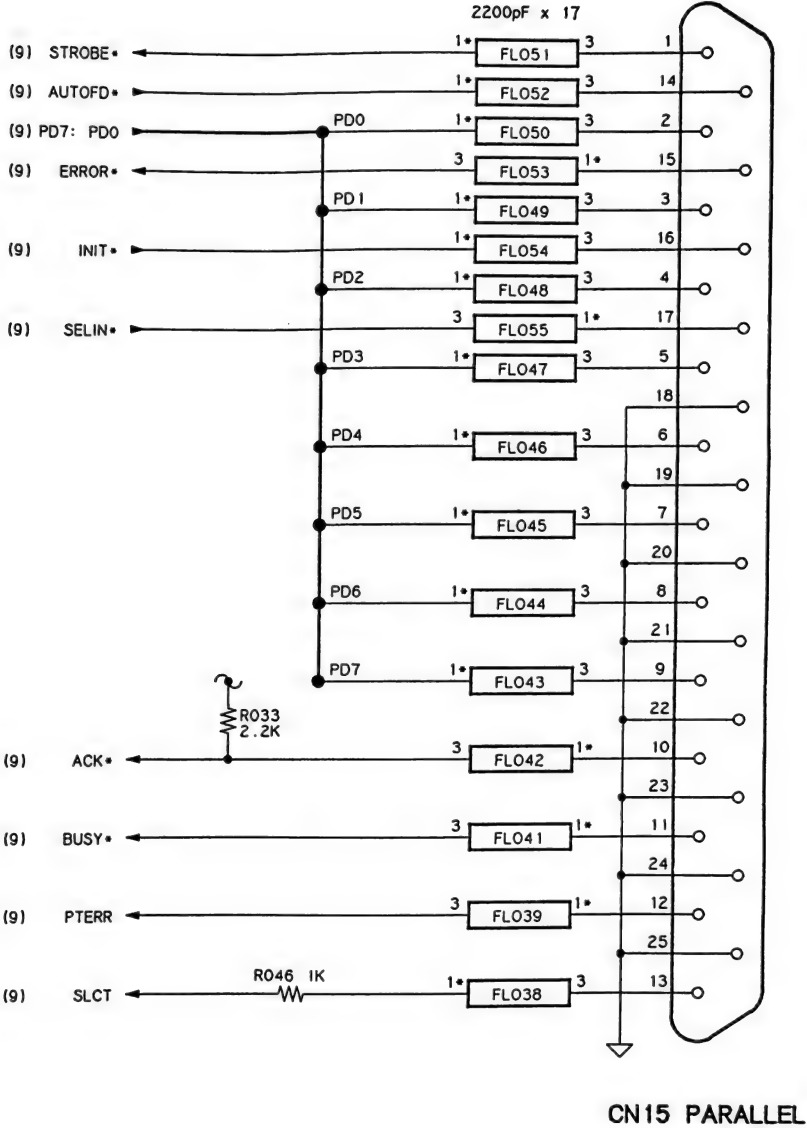
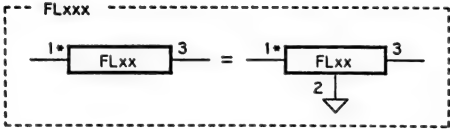
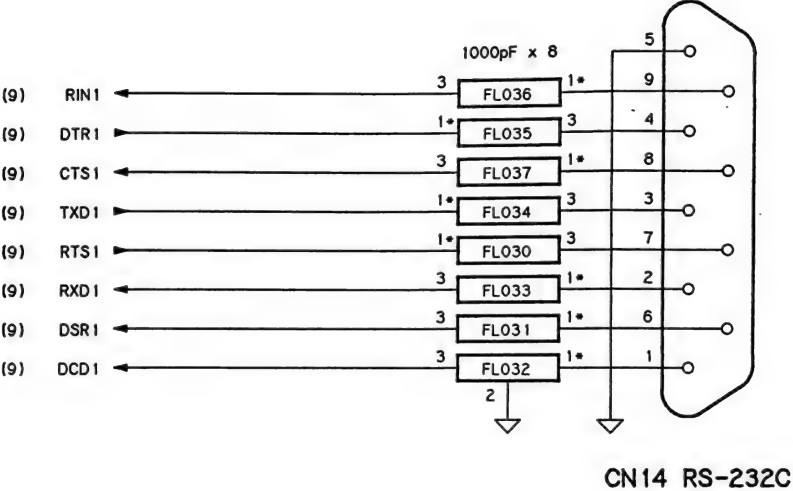
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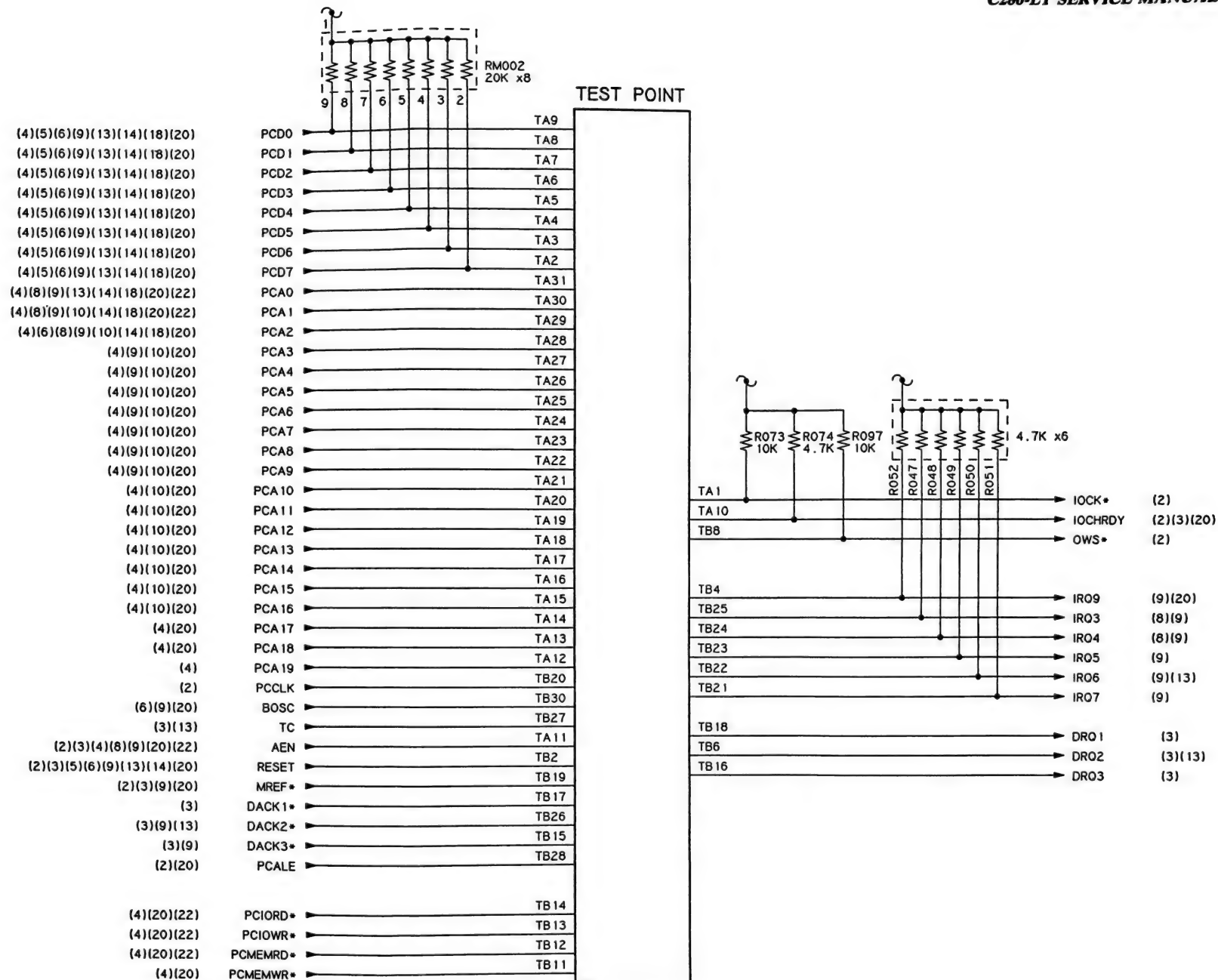
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1 MB	256Kx4	8	0.1
2 MB	1Mx4	4	0
* 4 MB	1Mx4	8	0.1

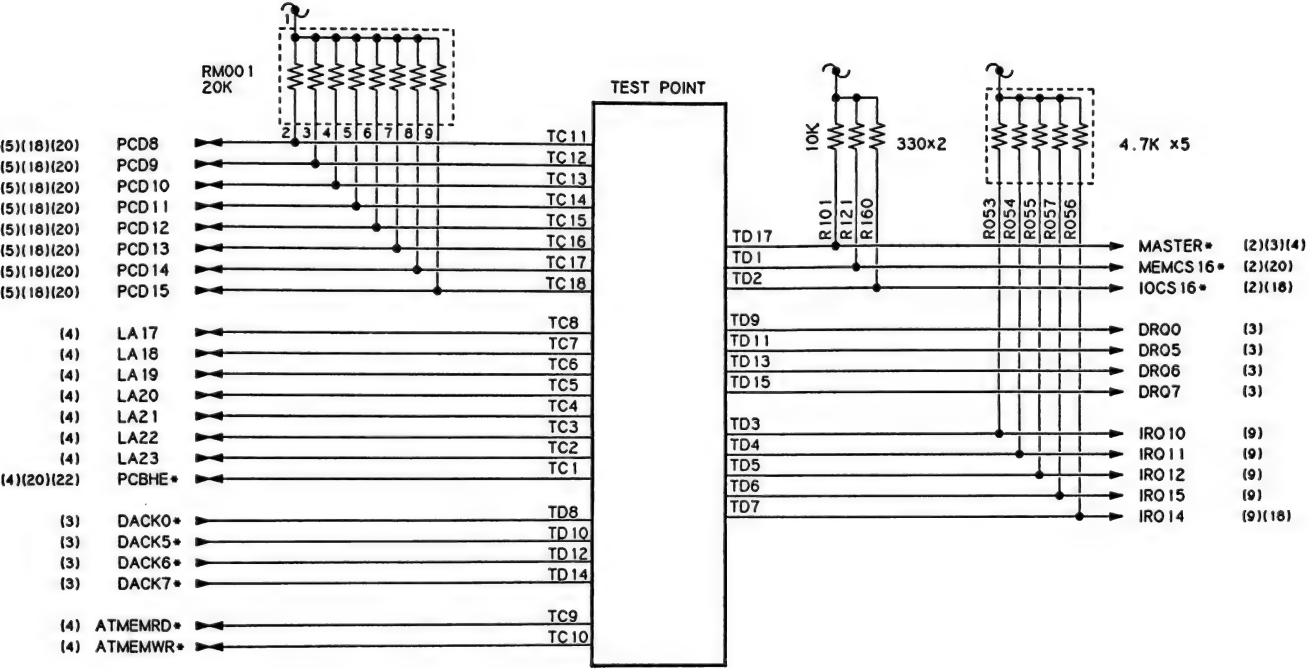


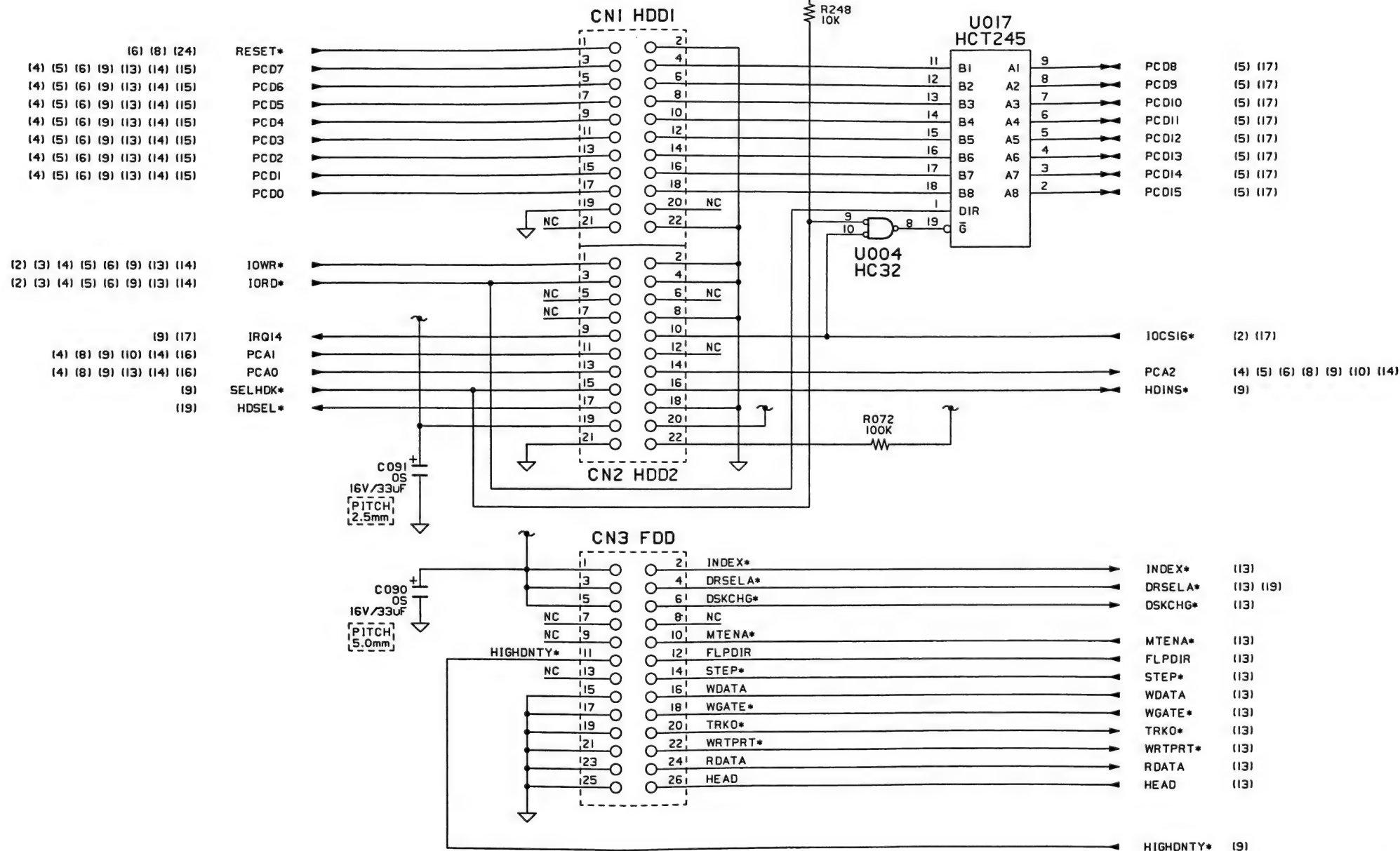




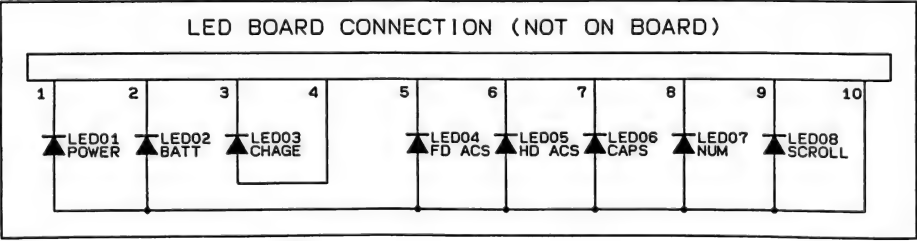
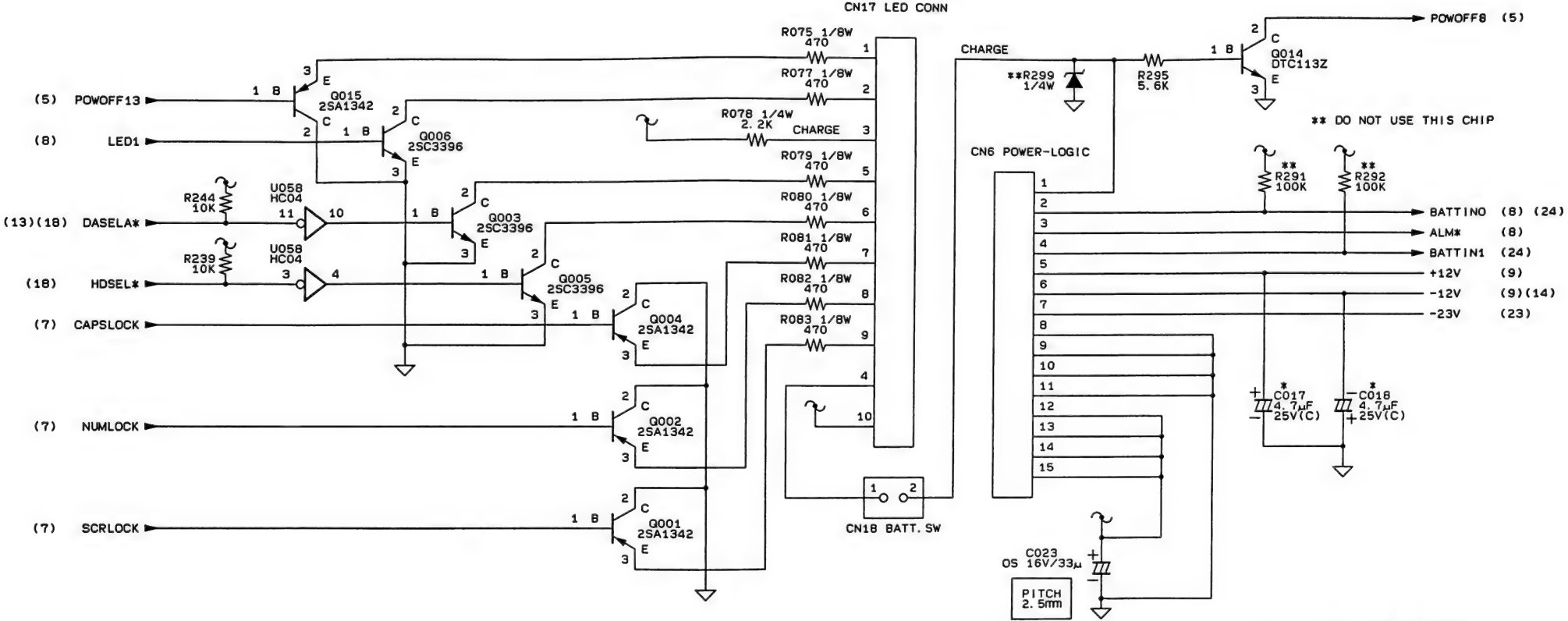
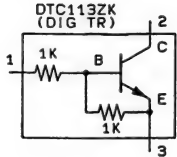
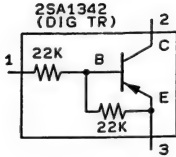
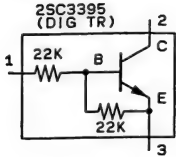




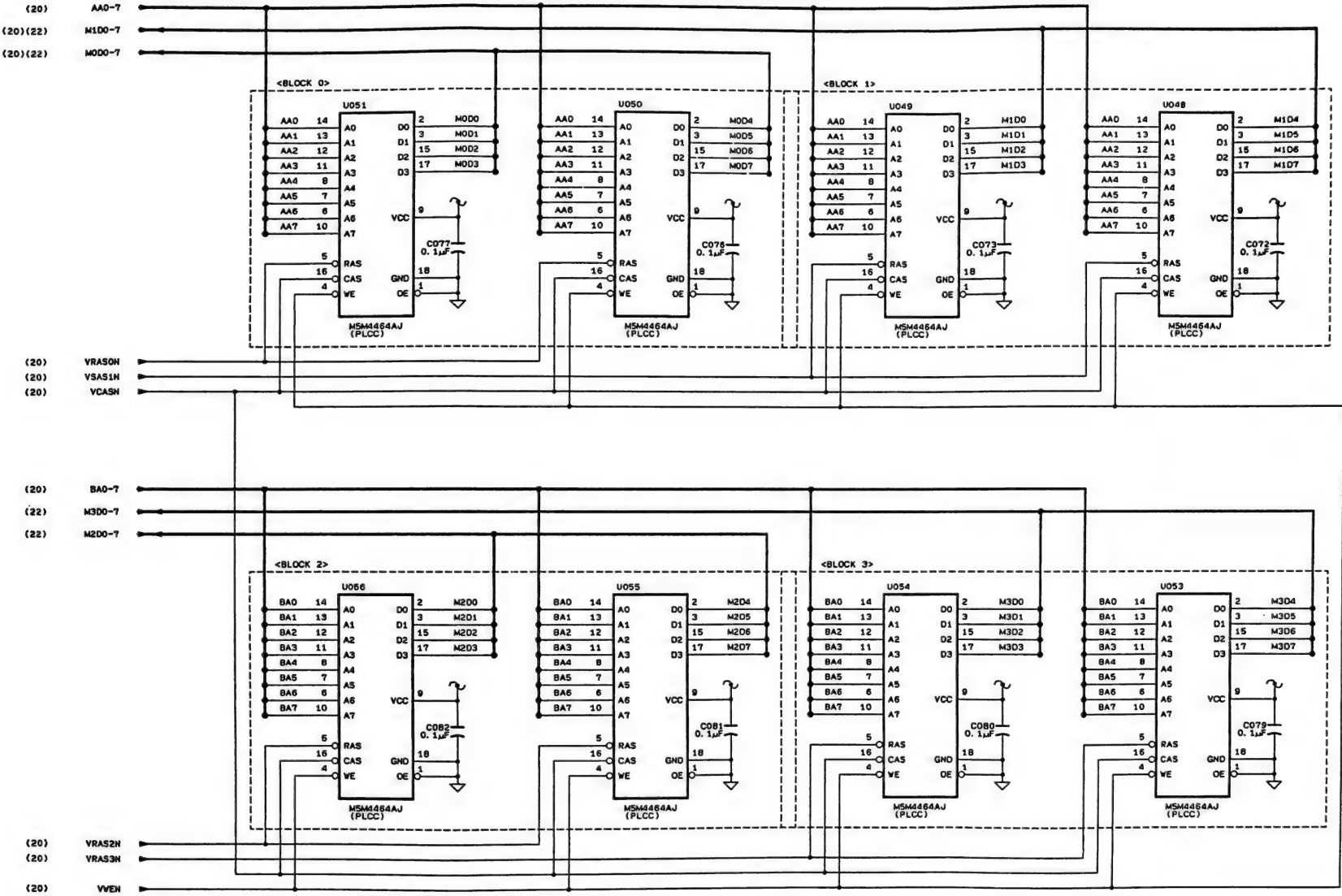


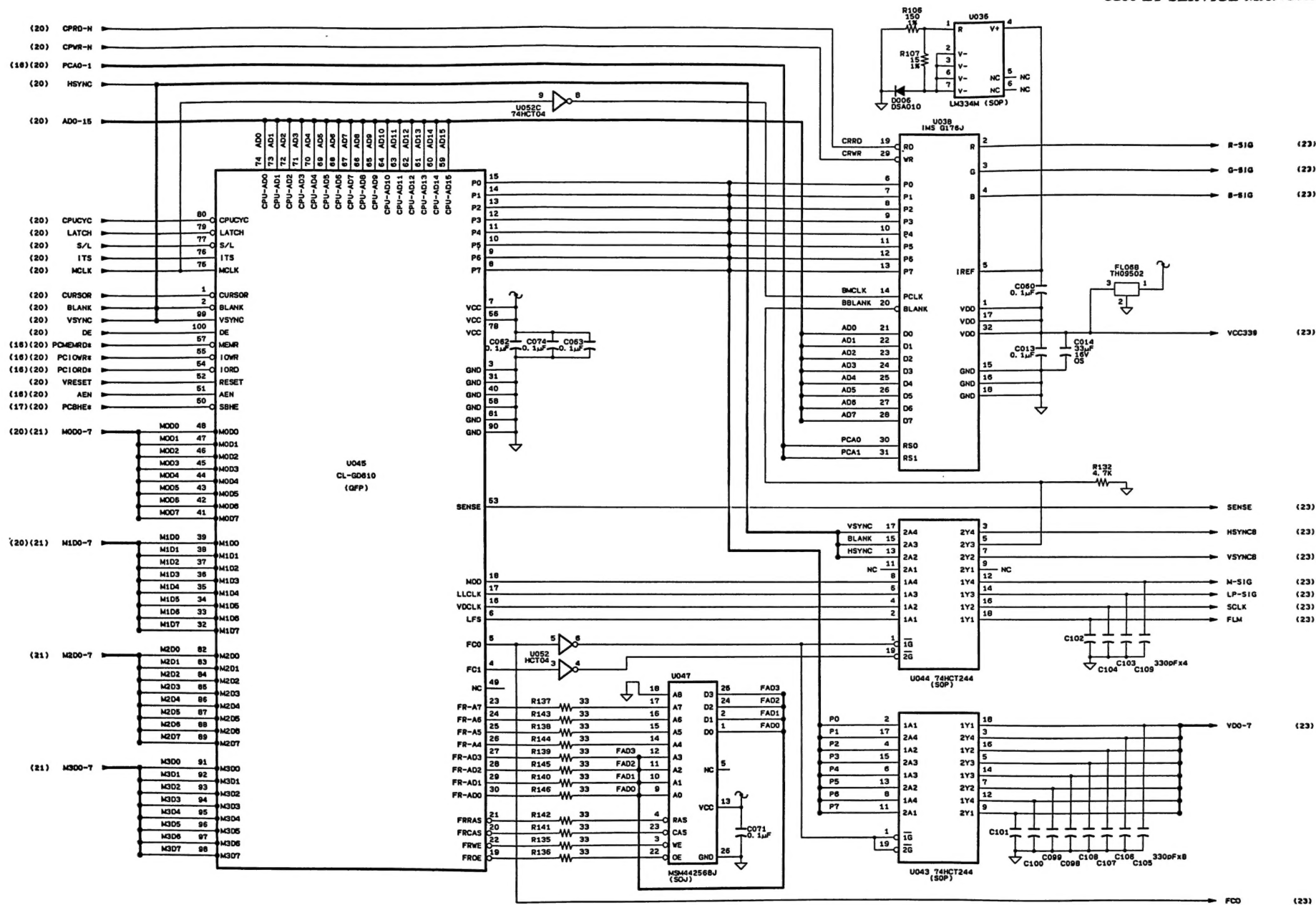


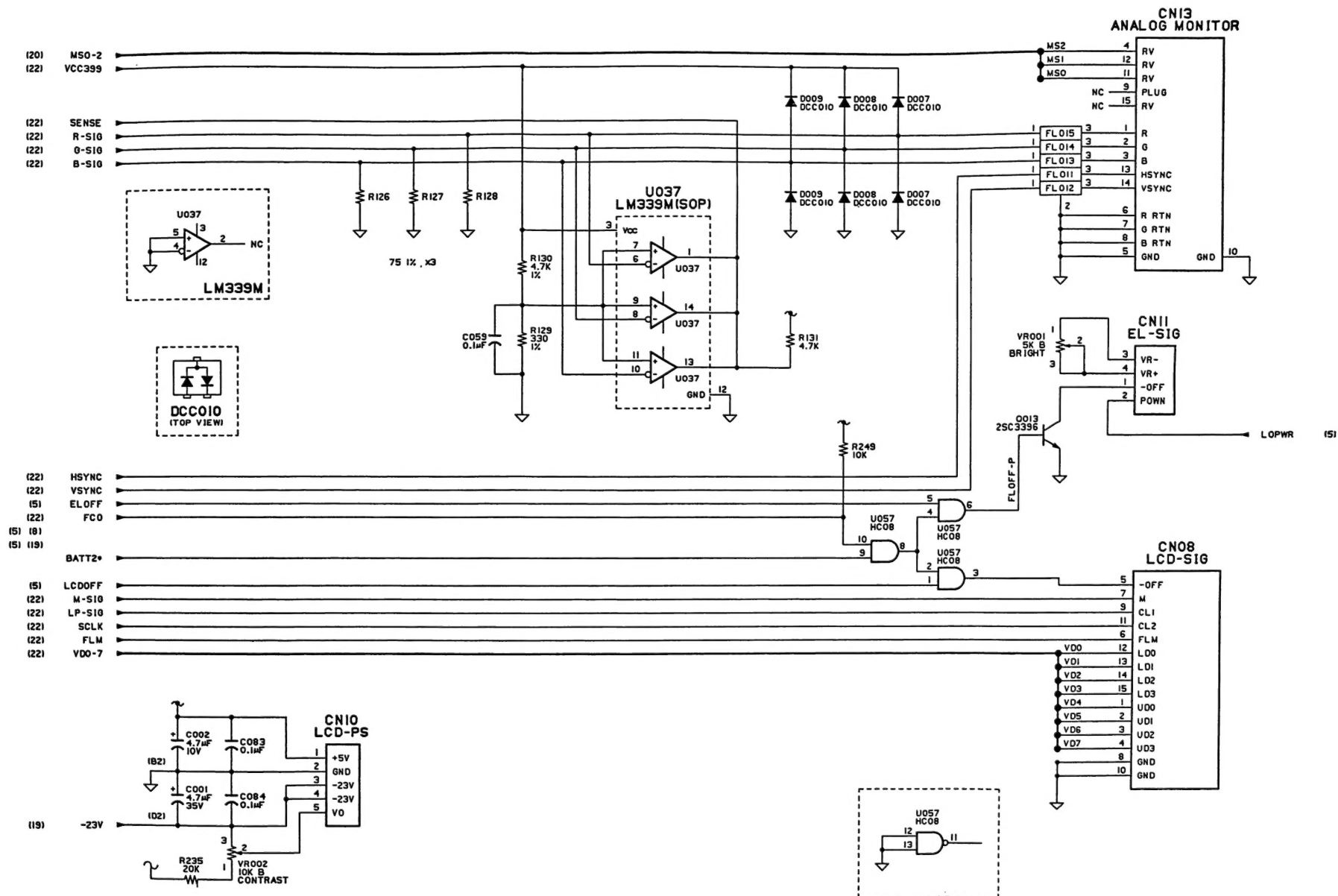


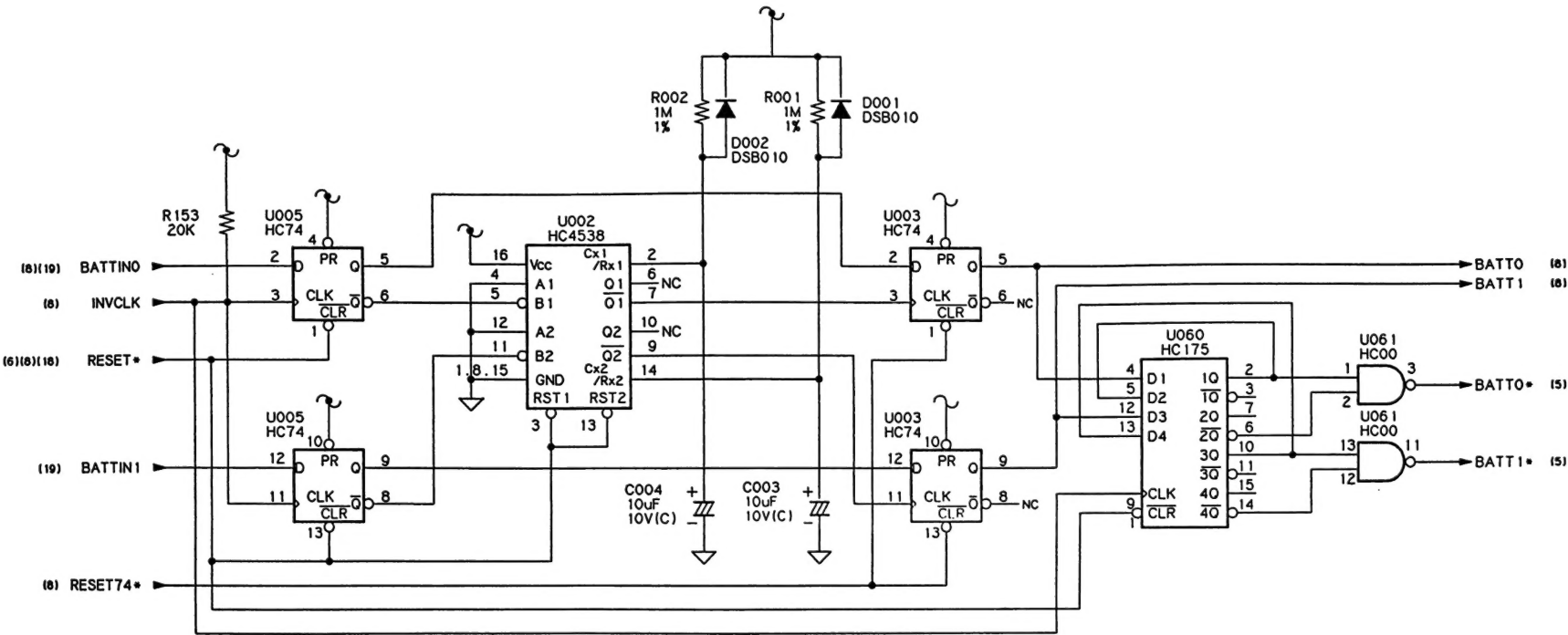














Computer Systems Division  
1200 Wilson Drive  
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